



on Fundamentals of Electronics, Communications and Computer Sciences

**VOL. E101-A NO. 2
FEBRUARY 2018**

**The usage of this PDF file must comply with the IEICE Provisions
on Copyright.**

**The author(s) can distribute this PDF file for research and
educational (nonprofit) purposes only.**

Distribution by anyone other than the author(s) is prohibited.

A PUBLICATION OF THE ENGINEERING SCIENCES SOCIETY



The Institute of Electronics, Information and Communication Engineers

Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3chome, Minato-ku, TOKYO, 105-0011 JAPAN

Two-Step Column-Parallel SAR/Single-Slope ADC for CMOS Image Sensors*

Hejiu ZHANG[†], Nonmember, Ningmei YU^{†a)}, Member, Nan LYU^{††}, and Keren LI[†], Nonmembers

SUMMARY This letter presents a 12-bit column-parallel hybrid two-step successive approximation register/single-slope analog-to-digital converter (SAR/SS ADC) for CMOS image sensor (CIS). For achieving a high conversion speed, a simple SAR ADC is used in upper 6-bit conversion and a conventional SS ADC is used in lower 6-bit conversion. To reduce the power consumption, a comparator is shared in each column, and a 6-bit ramp generator is shared by all columns. This ADC is designed in SMIC 0.18 μm CMOS process. At a clock frequency of 22.7 MHz, the conversion time is 3.2 μs . The ADC has a DNL of $-0.31/+0.38$ LSB and an INL of $-0.86/+0.8$ LSB. The power consumption of each column ADC is 89 μW and the ramp generator is 763 μW .

key words: A/D conversion, column-parallel ADC, SAR/single-slope ADC, CMOS image sensor

1. Introduction

Recently, the pixel size of CMOS image sensor (CIS) has decreased continuously and the pixel array has increased at the same time. As a result, the column-parallel analog-to-digital converter (ADC) has been widely used in CIS. In order to satisfy higher pixel resolution pictures and faster frame rate videos application requirements, it is necessary to investigate the high resolution and high conversion speed column-parallel ADC.

The single-slope (SS) ADC has been widely applied in the column-parallel architecture, because of its small area, high linearity and simple circuits [1]. However, the conversion speed of SS ADC is very slow, and limit its applications in high speed and high resolution CIS. To increase the A/D conversion speed, two-step ADCs based on SS have been proposed. Multiple-ramp single-slope (MRSS) ADC converts the input signal by a coarse phase with a ramp signal and a fine phase with multiple-ramp signals [2]. The conversion speed of MRSS is higher, but need more area and power consumption. To reduce the number of ramp, two-step SS ADCs with one or two ramp signals have been proposed [3], [4]. These ADCs have reduced the number of ramp generator and power consumption, and the conversion process is still divided into coarse and fine phase. The principle of SS-based ADC is simple, but the conversion speed is still

not high enough for high-speed and high-resolution CIS.

In order to obtain a higher A/D conversion speed, varieties of column-parallel ADC schemes have been studied. The successive approximation register (SAR) ADC achieves high conversion speed, but requires a large area for capacitor digital-to-analog converter (DAC). A column-parallel two-step SS/SAR ADC is reported in [5]. The quantization process is split into coarse phase based on SS ADC and fine phase based on SAR ADC, obtaining upper-bit and lower-bit respectively. A smaller capacitor array is needed for the low resolution SAR ADC, and the conversion speed significantly compared with other SS-based ADCs. But a lot of accurate voltage references are required for fine conversion, which lead to a high power consumption. [6] proposed a two-step SAR/SS ADC, the scheme achieved the same conversion speed as SS/SAR ADC without many voltage references. But this ADC is shared by multiple columns.

This letter proposes a hybrid two-step SAR/SS ADC in each column for high-speed CIS. The ADC sequentially converts each input signal to upper-bit and lower-bit using the SAR ADC and SS ADC. The remainder of the letter is organized as follows. Section 2 describes the structure and operating principle of the proposed SAR/SS ADC. Section 3 presents simulation results and compares it with other two-step ADCs. Finally, Sect. 4 concludes our research.

2. Proposed SAR/SS ADC

2.1 Architecture of the Proposed ADC

Figure 1 shows the architecture block diagram of proposed $(P+Q)$ -bit two-step column-parallel SAR/SS ADC for CIS. All m -column share a Q -bit ramp generator, a reference generator and a bias generator. Each column analog circuit

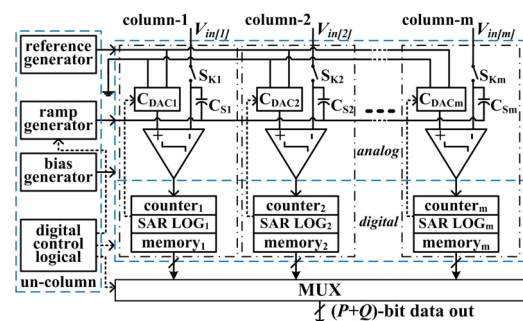


Fig. 1 Architecture of the column-parallel SAR/SS ADC.

Manuscript received May 12, 2017.

Manuscript revised August 21, 2017.

[†]The authors are with the Dept. of Electronic Engineering, Xi'an University of Technology, Xi'an, 710048 China.

^{††}The author is with the Dept. of Information Engineering, Xi'an University of Technology, Xi'an, 710048 China.

*This paper is supported by National Natural Science Foundation of China No.61471296 and No.61771388.

a) E-mail: yunm@xaut.edu.cn

DOI: 10.1587/transfun.E101.A.434

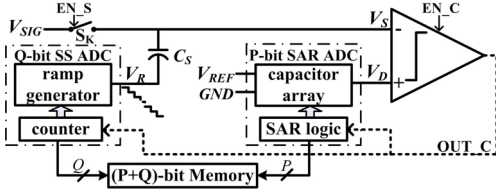


Fig. 2 Schematic of the single-column SAR/SS ADC.

consists of a shared comparator, a P -bit capacitor digital-to-analog converter (DAC) for P -bit SAR ADC and a sampling capacitor with a switch. An accurate voltage, generated by reference generator, and GND is used as P -bit capacitor DAC voltage references. The A/D conversion process is divided into upper P -bit and lower Q -bit using SAR ADC and SS ADC, respectively. In the end, the upper P -bit and the lower Q -bit are merged in memory, and $(P + Q)$ -bit data outputs by MUX.

The schematic of the proposed $(P + Q)$ -bit SAR/SS ADC is shown in Fig. 2. The input voltage V_{SIG} is sampled to the top plate of capacitance C_S by the control of signal EN_S . The ramp generator outputs a down ramp voltage V_R . V_{REF} and GND are used as reference voltage for P -bit capacitor DAC. The comparator is shared by the SAR ADC and SS ADC, and used to compare the output the DAC V_D with the top plate voltage of the sampling capacitance V_S . The output of the comparator OUT_C is the feedback signal for the SAR logic of the SAR ADC and the counter of the SS ADC. The final digital output is stored in $(P+Q)$ -bit memory.

2.2 Operation Principle of the Proposed ADC

The timing diagram of the proposed SAR/SS ADC is shown in Fig. 3. During the sampling phase: The pixel voltage signal is sampled on the top plate of the C_S by the control of the signal EN_S , while the bottom plate of the C_S is connected to the output of the ramp generator V_R . The V_{US} , equal to $V_{REF}/2^P$, is the least significant bit (LSB) of the SAR ADC, and is the initial voltage of ramp generator output. The range of the ramp is from V_{US} to 0 and the ramp step V_{LS} is $V_{REF}/2^{P+Q}$. V_{LS} is the LSB of the SS ADC. The V_R is retaining a constant voltage V_{US} at this moment. Meanwhile, and both top and bottom plates of the capacitor array are connected to GND.

Upper P -bit quantitative phase: For the first bit, the largest capacitor of capacitor array is connected from GND to V_{REF} , and the voltage V_D becomes $V_{REF}/2$ from GND. Then the comparator compares the sampled voltage V_{SIG} with $V_{REF}/2$, if the V_{SIG} is smaller than $V_{REF}/2$, the output of the comparator OUT_C will turn to high voltage from low. The rising edge feeds back to SAR logic, and the first bit in REG_U is 0, the largest capacitor connects from V_{REF} to GND. Otherwise, it would be 1, the largest capacitor remains connected to V_{REF} . The following is the second bit, the V_D decreases to $V_{REF}/4$ or increases to $3V_{REF}/4$ according to the first bit is 0 or 1, then V_D compares with the stored V_{SIG} to obtain the second bit. Similarly, the subsequent bits of

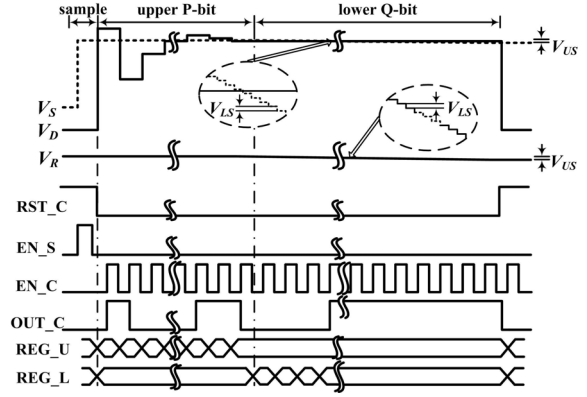


Fig. 3 Timing diagram of the proposed SAR/SS ADC.

the upper P -bit are obtained. The output value occurs in the P -bit register REG_U .

After the coarse conversion completes, the bottom plates of capacitor array are connected to GND or V_{REF} . The capacitor DAC output voltage V_D can be expressed as:

$$V_D = \sum_{i=1}^P \left(\frac{V_{REF}}{2^i} \cdot D_{SAR}[i] \right) \quad (1)$$

where $D_{SAR}[i]$ is the i -th bit of the coarse P -bit, i changes from 1 to P . If the last bit is 0, one clock period T_{clk} delay is needed for the V_D decreasing by V_{US} . When the coarse conversion completes, the V_D will always be less than V_S whether the last bit is 1 or not.

Lower Q -bit quantitative phase: The down ramp signal V_R , connected to the bottom plate of C_S , decreases step by step with the Q -bit counter increasing. The V_S changes as same as V_R , from V_{SIG} to $V_{SIG} - V_{US}$. Decreasing V_S compares with the constant V_D . When the V_S becomes less than V_D , the output of the comparator OUT_C will turn to high voltage from low. The register REG_L is continuously refreshed with the changing counter until the rising edge feeds back to counter. Finally, the lower Q -bit value is maintained in REG_L . In this process, V_S can be expressed as:

$$V_S = V_{SIG} - \frac{V_{REF}}{2^{P+Q}} \cdot j \quad (2)$$

where j is the comparing times of fine conversion, and changes from 1 to $2^Q - 1$. When A/D conversion process completes, values in REG_H and REG_L will be merged in $(P + Q)$ memory. The digital process is simple, and the total A/D conversion time T_{CONV} can be described as:

$$T_{CONV} = (P + 2^Q + 1) \cdot T_{clk} \quad (3)$$

2.3 Proposed 12-bit ADC

The conversion process of the proposed ADC is divided into upper P -bit and lower Q -bit by using SAR ADC and SS ADC, respectively. The P and Q are related to the performances of the ADC. The larger P value can achieve a higher

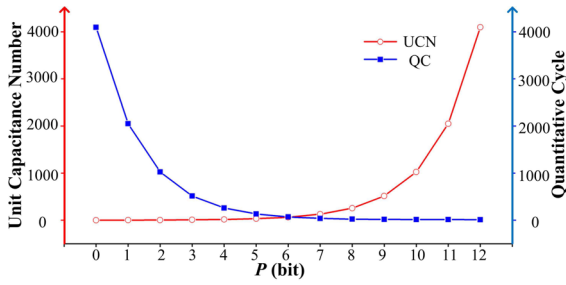


Fig. 4 The considerations of the bit number allocation.

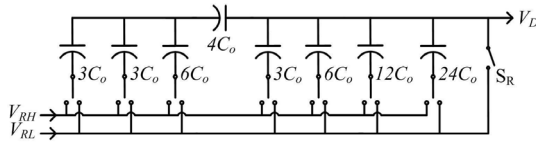


Fig. 5 The split capacitor array schematic diagram.

conversion speed, but a larger capacitor area and a major capacitor mismatch in the DAC. With the increase of Q value, the conversion time is exponentially increased. But, The SS ADC has a small area, high linearity and simple circuits. Therefore, reasonable allocation of upper bits (P) and lower bits (Q) can effectively balance the trade-off among the conversion time, capacitor area, mismatch and so on.

According to the P value, Fig. 4 shows the trends of unit capacitance number (UCN) and quantitative cycle (QC). When P is 6, UCN is 64 and QC is 70. Therefore, 6-bit SAR ADC for upper bits and 6-bit SS ADC for lower bits could get a better tradeoff between conversion time and unit capacitance number. The conversion speed is obviously improved, and the area fit for the column circuit application.

To reduce the area, a split-capacitor DAC (split-CDAC) is used in SAR ADC. In the split-CDAC, an $(H + L)$ -bit binary weighted capacitor array can be divided into an H -bit binary weighted capacitor array and an L -bit binary weighted capacitor array, and the bridge capacitor C_B should be:

$$C_B = \frac{2^L}{2^L - 1} \cdot C_U \quad (4)$$

where C_U is the unit capacitance [7]. C_B is not always easy to match with C_U in the traditional architecture. Here, the 6-bit binary weighted capacitor array is divided into a 4-bit binary weighted and a 2-bit binary weighted capacitor array, so that the bridge capacitor becomes easy to match with unit capacitance. As shown in Fig. 5, when unit capacitance C_U is designed as $3C_o$, the bridge capacitor will be $C_B = 4C_o$. The total capacitance for DAC is about 1.1 pF and the area is reduced to 30% of the original area.

3. Simulation Results

The proposed high-speed 12-bit SAR/SS ADC is designed in SMIC 0.18 μm CMOS process. At a clock frequency of 22.7 MHz, the A/D conversion time is 3.2 μs , less than 2% of conventional SS ADC. The capacitance for SAR ADC is

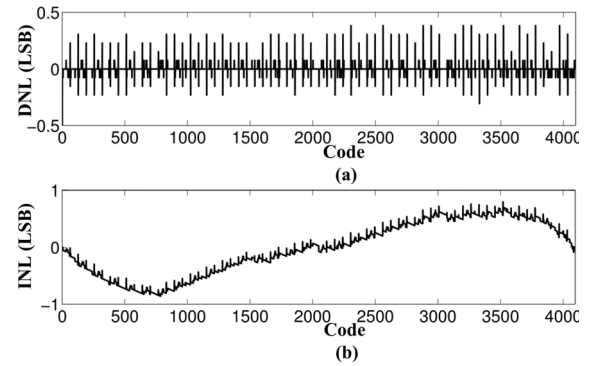


Fig. 6 The static characteristics of the proposed ADC (a) DNL (b) INL.

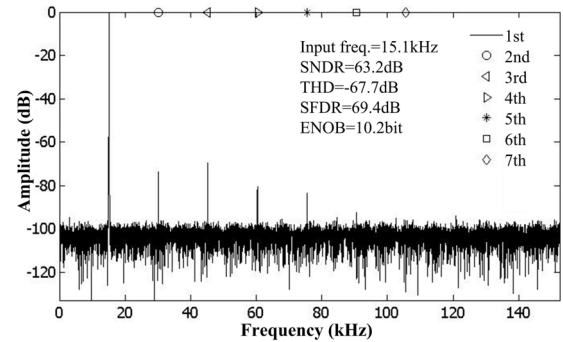


Fig. 7 FFT analysis of the proposed ADC.

about 1.1 pF and the area is reduced to 30% of the original area. The power consumption of each column ADC is 89 μW and the ramp generator is 763 μW . The figure-of-merit (FoM) is about 70 fJ/step. The FoM is defined as:

$$FoM = \frac{P_{ADC}}{2^N} \cdot T_{CONV} \quad (5)$$

where P_{ADC} is the ADC power consumption, N is defined as the ADC resolution and T_{CONV} is the A/D conversion time.

The static characteristics of the proposed 12-bit SAR/SS ADC are shown in Fig. 6. The simulated differential nonlinearity (DNL) and integral nonlinearity (INL) are $-0.31 / +0.38$ LSB and $-0.86 / +0.8$ LSB, respectively. The capacitor mismatch in DAC makes the step size of the upper 6-bit SAR ADC mismatch with the quantization range of the lower 6-bit SS ADC, and leads larger DNL glitches. Therefore, the glitches regularly appear when the lower 6-bit change from 111111 to 000000 (see Fig. 6(a)). The INL is the accumulation of the DNL, and the linear increasing or decreasing DNL leads to a large INL. To achieve a good INL, the quantization range of the lower 6-bit has been designed based on the Monte Carlo simulation of the upper bits SAR ADC step voltage. Therefore, the proposed ADC achieves a nonlinear INL (see Fig. 6(b)).

The fast fourier transformation (FFT) analysis results with a 15.1 kHz input frequency are shown in Fig. 7. The total harmonic distortion (THD), calculated from harmonics, is about -67.7 dB. The spurious free dynamic range (SFDR)

Table 1 Performance summary of the proposed ADC.

Process	0.18 μm CMOS
Resolution(bit)	12
Conv. time(μs)	3.2
DNL(LSB)	$-0.31 / +0.38$
INL(LSB)	$-0.86 / +0.8$
SNDR(dB)	63.2
SNR(dB)	65.1
SFDR(dB)	69.4
ENOB(bit)	10.2
ADC power(μW)	89
FoM(fJ/step)	70
Ramp power(μW)	763

Table 2 Comparison of previously two-step column-parallel architectures and this work.

Reference	[3]	[4]	[5]	[6]	This work
Frequency(MHz)	50	62.5	40	4	22.7
Resolution(bit)	10	12	11	9	12
Conv. time(μs)	6	6.4	12	3.3	3.2
Power(μW)	-	90	-	3	89
FoM(fJ/step)	-	-	41.7	37.8	70

is 69.4 dB, which could get from the 3rd harmonic. The signal-to-noise and distortion ratio (SNDR) is 63.2 dB. The effective number of bits (ENOB) is 10.2-bit, which is get from the formula:

$$SNDR = 6.02 \cdot ENOB + 1.76 \quad (6)$$

Table 1 summarizes the final performance of the designed SAR/SS ADC. Table 2 compares the simulated results of proposed ADC with previously two-step column-parallel architectures. The proposed ADC has a higher conversion speed and achieves a lower power consumption compared to the two-step SS-based ADC in [3], [4]. Compared with ADC in [5], the proposed ADC doesn't need some accurate voltage references with corresponding buffers for SAR conversion. The ADC is shared by multiple columns in [6], the CIS row conversion time is the ADC conversion time multiply by the numbers of share ADC columns. Therefore, the proposed

ADC could achieve a higher frame frequency. In addition, it has more capacitance and lower resolution compare with the proposed ADC.

4. Conclusion

A two-step column-parallel 12-bit SAR/SS ADC for CIS is proposed in this letter. The quantization process is divided into coarse upper 6-bit SAR ADC and fine lower 6-bit SS ADC. A split-CDAC is used in SAR ADC and the area is reduced to 30% of the original area. A 6-bit ramp generator is designed for SS ADC. At a clock frequency of 22.7 MHz, the A/D conversion time is 3.2 μs . The power consumption of each column ADC is 89 μW and the ramp generator is 763 μW .

References

- [1] D. Kim and M. Song, "An enhanced dynamic-range CMOS image sensor using a digital logarithmic single-slope ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol.59, no.10, pp.653–657, Oct. 2012.
- [2] M.F. Snoeijs, A.J.P. Theuvsen, K.A.A. Makinwa, and J.H. Huijsing, "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," *IEEE J. Solid-State Circuits*, vol.42, no.12, pp.2968–2977, Dec. 2007.
- [3] N. Lyu, N. Yu, and H. Zhang, "A high-speed column-parallel time-digital single-slope ADC for CMOS image sensors," *IEICE Trans. Fundamentals*, vol.E99-A, no.2, pp.555–559, Feb. 2016.
- [4] J. Lee, H. Park, B. Song, K. Kim, J. Eom, K. Kim, and J. Burm, "High frame-rate VGA CMOS image sensor using non-memory capacitor two-step single-slope ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.62, no.9, pp.2147–2155, Sept. 2015.
- [5] F. Tang, D.G. Chen, B. Wang, and A. Bermak, "Low-power CMOS image sensor based on column-parallel single-slope/SAR quantization scheme," *IEEE Trans. Electron Devices*, vol.60, no.8, pp.2561–2566, Aug. 2013.
- [6] D.G. Chen, F. Tang, M.K. Law, and A. Bermak, "A 12 pJ pixel analog-to-information converter based 816 \times 640 pixel CMOS image sensor," *IEEE J. Solid-State Circuits*, vol.49, no.5, pp.1210–1222, May 2014.
- [7] J.Y. Um, Y.J. Kim, E.W. Song, J.Y. Sim, and H.J. Park, "A digital-domain calibration of split-capacitor DAC for a differential SAR ADC without additional analog circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.60, no.11, pp.2845–2856, Nov. 2013.