A Novel Active Gate Driver for Improving Switching Performance of High-Power SiC MOSFET Modules

Yuan Yang, Yang Wen, and Yong Gao

***Abstract*—Featuring higher switching speed and lower losses, the silicon carbide MOSFETs (SiC MOSFETs) are widely used in higher power density and higher efficiency power electronic applications as a new solution. However, the increase of the switching speed induces oscillations, overshoots, electromagnetic interference (EMI), and even additional losses. In this paper, a novel active gate driver (AGD) for high-power SiC MOSFETs is presented to fully utilize its potential of high-speed characteristic under different operation temperatures and load currents. The principle of the AGD is based on drive voltage decrement during the voltage and current slopes since high *dV/dt* and *dI/dt* are the source of the overshoots, oscillations, and EMI problems. In addition, the optimal drive voltage switching delay time has been analyzed and calculated considering a tradeoff between switching losses and switching stresses. Compared to conventional gate driver with fixed drive voltage, the proposed AGD has the capability of suppressing the overshoots, oscillations, and reducing losses without compromising the EMI. Finally, the switching performance of the AGD was experimentally verified on 1.2 kV/300 A and 1.7 kV/300 A SiC MOSFETs in double pulse test under different operation temperatures and load currents. In addition, an EMI discussion and cost analysis were realized for AGD.**

***Index Terms*—Active gate driver (AGD), electromagnetic interference (EMI), silicon carbide (SiC) MOSFET, overshoots.**

I. Introduction

With rapid development of the power electronic technology, more and more applications pose new demands on power devices [1]–[3], e.g., higher current and voltage, increased power density, and higher efficiency. Featuring higher switching frequency, higher thermal conductivity, increased operation temperature, and lower switching and conduction loss, silicon carbide MOSFETs (SiC MOSFETs) serving as a solution are expected to be gradually used to meet these requirements [4], [5]. However, overshoots, oscillations and electromagnetic interference (EMI) induced by faster switching speed and parasitic elements are the key obstacles to its wide applications.

A. Overshoots

In applications, the parasitic elements in the power devices and converter circuits cannot be eliminated. When a power device works in high frequency, the *dI/dt* and *dV/dt* slopes are increased due to stray inductances and parasitic capacitances, which leads to the overshoots in current and voltage [6]–[9]. When the voltage and current overshoots exceed the breakdown voltage of the SiC MOSFETs and maximum recovery current of the freewheeling diode, the devices will be destroyed.

B. Oscillations

The switching oscillation, or ringing phenomenon, was observed in many SiC device studies [10]–[13]. The same phenomenon was also observed in high-frequency silicon MOSFET and insulated-gate bipolar transistor applications [14]. The switching oscillation phenomenon is closely related to the fast switching characteristics of the power switches. The high *dV/dt* and *dI/dt* of SiC MOSFETs during switching transient accompanied with the parasitic elements in the circuit are responsible for the oscillations.

C. EMI

When a power SiC MOSFET working in high frequency, the EMI problems, which decrease the performance, will be present due to high switching speed and stray inductances [9], [12], [15]–[17].

The aforementioned issues are typically addressed from four viewpoints, each has its limitations for SiC MOSFETs.

1) Slowdown of the Switching Speed: Slowdown of the switching speed with high gate resistance can obviously alleviate the switching stress and oscillations, and suppress the EMI [18]–[20]. However, the decrement of the switching speed brings more switching loss and prolongs the switching time.

2) Additional RC Snubber Circuit: Adding RC snubber circuits to suppress the switching stress is a common method [10], [21]–[23]. In [21], the RC snubber circuits are used to dampen the ringing during switching transient in buck converters. The same idea of adding an RC snubber across the power supply bus or placing a ferrite bead in the power loop is also reported in [22]. Other solutions applying snubber circuits have reached better performance in Si and SiC devices [23]. Nevertheless,

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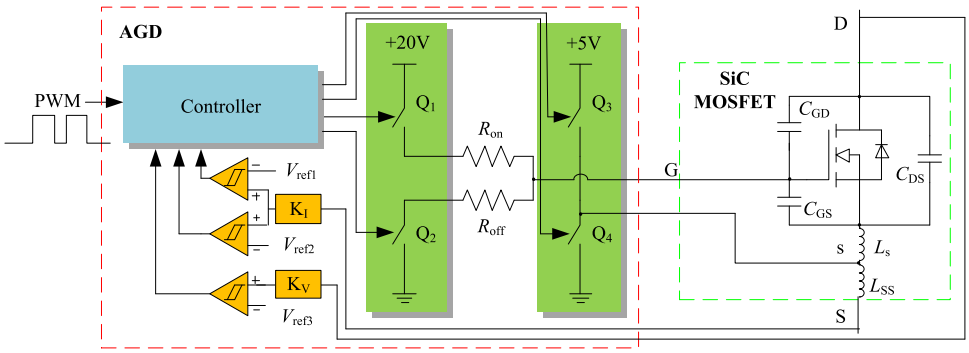


Fig. 1. General scheme of the proposed AGD.

these circuits can leave high stress in additional components, such as inductors and capacitors. On the other hand, the additional huge components increase the energy losses and decrease the efficiency.

3) Optimization of the Layout: Optimizing packaging of the power devices and reducing stray inductance in power loops are two major research directions for the layout optimization [24]–[29]. Some scholars have been working on the research of new packaging technology [24]–[27]. Additionally, when using a better design of PCB layout, the stray inductance will be reduced, and the EMI problems can also be lower [28], [29]. However, the latest packaging technology is always expensive and will take a long time to be commercialized. In addition, the stray inductance in high-power applications is difficult to reduce due to the complex structure and high cost. Therefore, the task to fully utilize the potential of SiC MOSFETs and improve the switching performance is focused on the advanced gate driver circuits.

4) Active Gate Driver as a Solution: A novel gate drive solution with multistage gate resistance was introduced in [30] and [31].The main advantage of this gate driver is the reduction of oscillations and overshoots. However, the switching loss is increased at the same time. Similarly, a gate driver with a timing resolution and range of output resistance was presented in [32]. Although the gate driver maintains a low switching loss of constant-strength gate driving while reducing overshoot, oscillation, and EMI, but it results in a complex circuit implementation since the bypass switches utilized to adjust the gate resistance are implemented by MOSFET. Besides, the thresholds calculation and setting method for pursuing an optimal switching performance is complex and inflexible for different power devices. A resonant damping circuit to suppress the switching ringing of full SiC MOSFET was proposed in [33]. The ringing is damped out by using air core PCB transformer which has a properly designed secondary side circuit. However, the main disadvantage is that the parameters calculation of the transformer is complicated and an additional PCB is required. A gate driver featuring *dV/dt* and *dI/dt* control for SiC MOSFETs turn-OFF was introduced in [34]. Experimental results showed that it can eliminate the overvoltage and reduce the turn-OFF loss. However, the turn-ON transient is not taken into consideration. In addition, laser devices are needed, which increased the cost. In [35], a closed-loop control gate driver was proposed, which can independently adjust the switching *dV/dt* and *dI/dt* by closed-loop control of the gate current and enable one to reach optimal performance in terms of loss, device stress, and EMI. However, the implementation of the circuits is complex and expensive for high performance analog amplifiers are utilized. Besides, the performance of the closed-loop system is deeply affected by the temperature of the SiC MOSFET modules and load current changes.

In this paper, a novel and simple active gate driver (AGD) is proposed to effectively suppress the overshoots, oscillations, and reduce losses without compromising the EMI. The main strategy of the proposed AGD is to reduce the current and voltage slope by decreasing gate drive voltage since high *dV/dt* and *dI/dt* are the source of the overshoots, oscillation, and EMI problems. Compared with previous works on SiC MOSFET gate driver, the proposed method features simple circuit implementation with no negative drive voltage and provides a flexible control, which permits an optimal tradeoff between overshoot and switching losses under different operation temperatures and load currents. This paper is organized as follows. In Section II, the AGD and operation principles are introduced in detail. The implementation and a prototype of the AGD are presented in Section III. Subsequently, the performance of the AGD is experimentally verified on high-power SiC MOSFET modules by double pulse test in Section IV and the switching performance of the AGD was analyzed and discussed in Section V. Finally, conclusions of this paper are given in Section VI.

II. AGD and Operation Principle

In this section, general schematic circuit and operation principle of the proposed AGD will be introduced in detail. The AGD circuit mainly consists of three parts as depicted in Fig. 1.

1) Gate drive stage: Four switches combined to achieve multi-voltage to actively control the SiC MOSFET.
2) Detection circuits: Three high-speed comparators used to detect drain current I_D signal and drain-source $V_{\rm DS}$ signal and clipping circuits (K_I, K_V) are utilized to guarantee a safe input voltage.
3) Controller: A Complex Programmable Logic Device (CPLD) is utilized to provide simple logical control.

In addition, the model of SiC MOSFET including junction capacitances ($C_{\rm GD}$, $C_{\rm GS}$, $C_{\rm DS}$) and module intrinsic parasitic inductances (L_s, $L_{\rm SS}$) is also depicted in the Fig. 1. The principle of the proposed AGD is to decrease the gate driver voltage value during the current and voltage slope. Thus, the gate current and

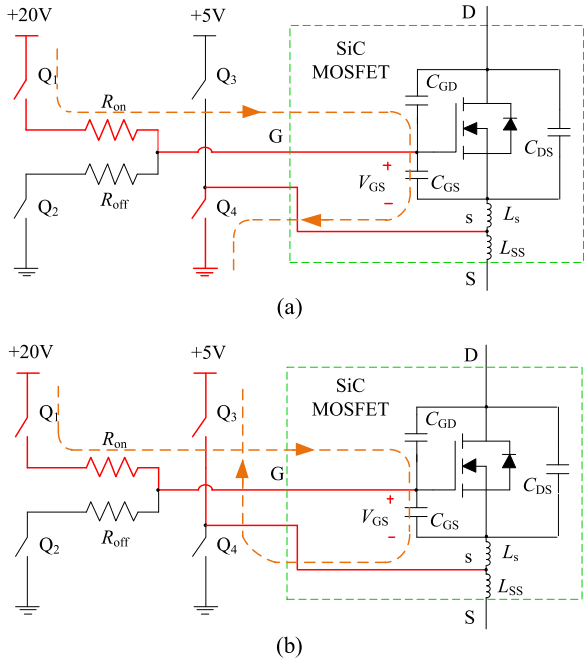


Fig. 2. Operation modes of the AGD at turn-ON. (a) 20 V generating circuit. (b) 15 V generating circuit.

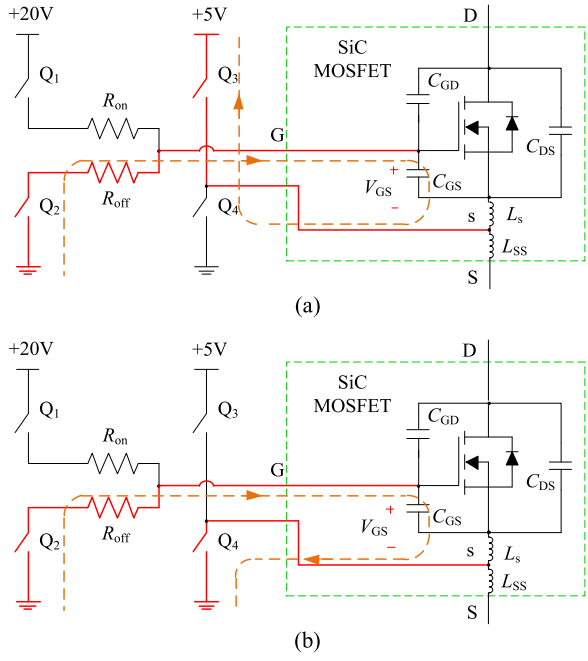


Fig. 3. Operation modes of the AGD at turn-OFF. (a) −5 V generating circuit. (b) 0 V generating circuit.

energy are reduced in this interval to suppress the overshoots and oscillations provoked by high *dV/dt* and *dI/dt*. The detailed operation principle of the proposed AGD will be introduced in the following.

A. Operation Modes

In order to obtain the recommended gate drive voltage (i.e., 20 V/−5 V) given in SiC MOSFETs' datasheet, in this design, 20 and 5 V are selected as the power supplies and four gate drive voltages (i.e., 20, 15, 0, and −5 V) are generated by the proposed AGD. Therefore, 15 and 0 V serving as the intermediate voltage are utilized to optimize the switching performance of SiC MOSFETs. As shown in Fig. 2, turn-ON gate control circuit is composed of two operation modes to generate gate drive voltages of 20 and 15 V, respectively. The implementation of the 20 V is achieved by activating switches Q_1 and Q_4. While, the 15 V is achieved by activating switches Q_1 and Q_3. Similarly, two operation modes are implemented to control turn-OFF transient as shown in Fig. 3. By the combination of the switches Q_2, Q_3, and Q_4, two gate drive voltages (i.e., −5 and 0 V) are achieved at turn-OFF transient. Since the SiC MOSFET is gate controlled device, its switching behavior can be actively improved by applying different gate drive voltage.

B. Operation Principle

1) Turn-ON Control Strategy: Fig. 4 shows the typical waveforms of turn-ON transient. When pulsewidth modulation (PWM) signal goes to high at t_0, Q_1 and Q_4 switches are activated and a high value gate drive voltage V_{GG} of 20 V is applied to the SiC MOSFET. Then, a high gate current is generated to charge the input capacitance $C_{iss} = C_{GS} + C_{GD}$ with R_{on} and V_{GS} starts to rise. When V_{GS} reaches the threshold

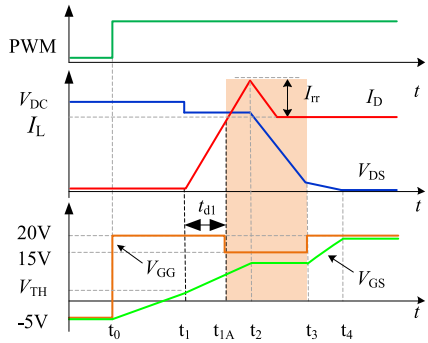


Fig. 4. Typical turn-ON waveforms of SiC MOSFET and output of the AGD.

voltage V_{TH} at t_1, the I_D begins to conduct. After a time delay t_{d1}, the Q_1 and Q_3 switches are activated at t_{1A}, a lower gate current is generated due to the lower gate voltage V_{GG} of 15 V. In this interval, I_D reaches the level of the load current I_L and V_{GS} reaches the Miller plateau voltage. On the other hand, the V_{DS} starts to fall and a peak of current occurs due to the freewheeling diode effect. When the V_{DS} drops below $0.1V_{DC}$ at t_3, the Q_1 and Q_4 switches are reactivated and the V_{GS} starts to rise again. Finally, the SiC MOSFET fully conducts at t_4. The current slope of I_D during the turn-ON transient is approximated from the following equation:

$$\frac{dI_D}{dt} = \frac{V_{GG} - V_{TH} - \frac{I_D}{g_m}}{\frac{C_{iss} \cdot R_{on}}{g_m} + L_s} \tag{1}$$

where g_m is the transconductance of the SiC MOSFET.

On the other hand, the voltage slope can be calculated as

$$\frac{dV_{DS}}{dt} = -\frac{V_{GG} - V_{Miller}}{C_{GD} \cdot R_{on}} \tag{2}$$

where C_{GD} is the gate-drain capacitance of the SiC MOSFET.

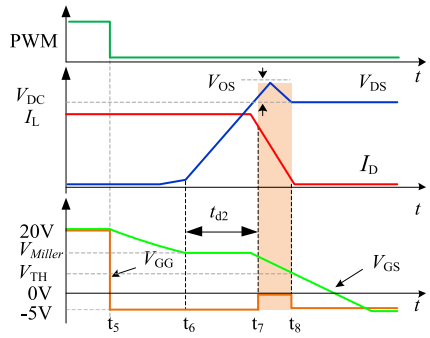


Fig. 5. Typical turn-OFF waveforms of SiC MOSFET and output of the AGD.

According to (1) and (2), the current and voltage slopes at turn-ON transient can be adjusted by applying different positive gate drive voltage.

2) Turn-OFF Control Strategy: The typical turn-OFF waveforms of SiC MOSFETs are shown in Fig. 5. When PWM signal goes to low at t_5, Q_2 and Q_3 switches are activated and a negative voltage (i.e., -5 V) is generated to discharge the $C_{\rm iss}$ with $R_{\rm off}$. $V_{\rm GS}$ starts to fall from 20 V until it drops to voltage Miller at t_6 and $V_{\rm DS}$ rises rapidly. After a delay time t_{d2}, Q_2 remains ON, Q_3 is turned OFF, and Q_4 is turned ON, 0 V is generated until the I_D is completely turned OFF at t_8. During this interval, a voltage overshoot occurs due to the falling of I_D and the existing stray inductance in power loop. After t_8, Q_2 and Q_3 switches are activated again generating a gate voltage far below the $V_{\rm TH}$ to prevent the turn-ON of the SiC MOSFET in OFF-state. The voltage slope can be calculated as

$$\frac{dV_{\rm DS}}{dt} = \frac{V_{\rm GG} - V_{\rm Miller}}{C_{\rm GD} \cdot R_{\rm off}}. \tag{3}$$

The current slope of I_D during the turn-OFF transient is approximated from the equation

$$\frac{dI_D}{dt} = g_m \cdot \frac{V_{\rm TH} + \frac{I_D}{g_m} - V_{\rm GG}}{\frac{C_{\rm iss} \cdot R_{\rm off}}{g_m} + L_s}. \tag{4}$$

According to (3) and (4), the current and voltage slopes at turn-OFF transient can be adjusted by applying different negative gate drive voltage.

III. Implementation of the AGD

According to the Fig. 1, the AGD mainly consists of three parts: gate drive stage, detection circuits, and CLPD. Detailed circuits of the proposed AGD were implemented as shown in Fig. 6.

A. Implementation of the Gate Drive Stage

As introduced in Section II, the implementation of the gate drive stage circuit mainly relies on the four switches. In this design, two ultrafast MOSFET drivers IXDN609 from IXYS corporation were chosen to implement the gate drive stage circuit. On one hand, it has a totem pole structure inside. On the other hand, it features wide operating voltage range (i.e., 4.5 to 35 V) and high peak source/sink drive current (i.e., 9 A). These characteristics are particularly suitable for this design.

B. Implementation of the Detection Circuits

In order to successfully implement the multi-voltage switching strategy, different switching stages of SiC MOSFET should be detected accurately. There are three signals that can be utilized to detect the different switching stages of SiC MOSFET: the turn-ON/ turn-OFF command signal, I_D, and $V_{\rm DS}$.

For the I_D detection, the voltage across the source inductance $V_{\rm SS}$ is utilized as $V_{\rm SS} = L_{\rm SS} * dI_{\rm D}/dt$. In addition, two individual blocks are adopted to capture the positive and negative drain current slopes ($V_{\rm SS}$), respectively. At turn-ON transient, as soon as the I_D starts to rise, a negative $V_{\rm SS}$ turns ON the transistor T_1 and pulls down the input voltage of the comparator CP_2 below the reference voltage $V_{\rm ref2}$. As a consequence, CP_2 sends a falling edge signal to the CLPD. At turn-OFF transient, when the I_D starts to fall, a positive voltage $V_{\rm SS}$ is firstly scaled-down by resistor R_5 and R_6 and is then sent to CP_1. Once the input value rises beyond the reference voltage $V_{\rm ref1}$, a rising edge signal will be sent from CP_1 to the CLPD. As soon as the I_D drops below zero, the positive voltage $V_{\rm SS}$ drops below the reference voltage $V_{\rm ref2}$, a falling edge signal will be sent from CP_1 to the CLPD. Therefore, the value of $V_{\rm ref1}$ and $V_{\rm ref2}$ can be determined, respectively, by the following equations:

$$V_{\rm ref1} = \frac{R_6}{R_5 + R_6} \cdot V_{\rm SS(+)} \tag{5}$$

$$V_{\rm ref2} = 5 + \frac{R_3}{R_4}\left(V_{\rm SS(-)} + V_{\rm BE}\right) \tag{6}$$

where $V_{\rm SS(+)}/V_{\rm SS(-)}$ is positive/negative threshold values of the $V_{\rm SS}$ and $V_{\rm BE}$ is the base-emitter voltage of the transistor T_1.

For the $V_{\rm DS}$ detection, $V_{\rm DS}$ is first scaled by an *RC* divider with a factor K_1, which should be selected to ensure that the signal $K_1 * V_{\rm DS}$ must be limited within the maximum input value of the CP_3. As soon as the $K_1 * V_{\rm DS}$ drops below V_{ref3} at turn-ON transient, a high-to-low signal edge from CP_3 will be sent to the complex programmable logic device (CPLD). On the contrary, when the $K_1 * V_{\rm DS}$ exceeds $V_{\rm ref3}$ at turn-OFF transient, a low-to-high signal edge from CP_3 will be sent to the CLPD. Thus, the value of $V_{\rm ref3}$ can be determined by

$$V_{\rm ref3} = K_1 \cdot V_{\rm DS(th)} = \frac{R_7}{R_7 + R_8} \cdot V_{\rm DS(th)} \tag{7}$$

where $V_{\rm DS(th)}$ is the threshold values of the $V_{\rm DS}$.

Ideally, $V_{\rm SS(+)}$, $V_{\rm SS(-)}$, and $V_{\rm DC(th)}$ is zero. In practice, when these thresholds are too close to zero or the scaling factors of the clipping circuits are too small, it would be false triggered by jitter or oscillation of the signals. However, when these parameters are set large enough, the delay time of the AGD is increased and the switching accuracy is reduced. Therefore, the value of the $V_{\rm SS(+)}$, $V_{\rm SS(-)}$, and $V_{\rm DC(th)}$ should be selected carefully as these parameters affect the switching performance of the AGD. According to the experience, in this design, $V_{\rm SS(+)}/V_{\rm SS(-)}$ is set as $\pm 0.1\, V_{\rm SS}$ and $V_{\rm DC(th)}$ is set as $0.1 V_{\rm DC}$.

Two falling edge signals from CP_1 and CP_2 are utilized to indicate the start and the end of I_D at switching transient, respectively, and the falling and rising edge signal from CP_3 indicate the end and start of the $V_{\rm DS}$ at switching transient, respectively. With these four signals, the core controller can accurately recog-

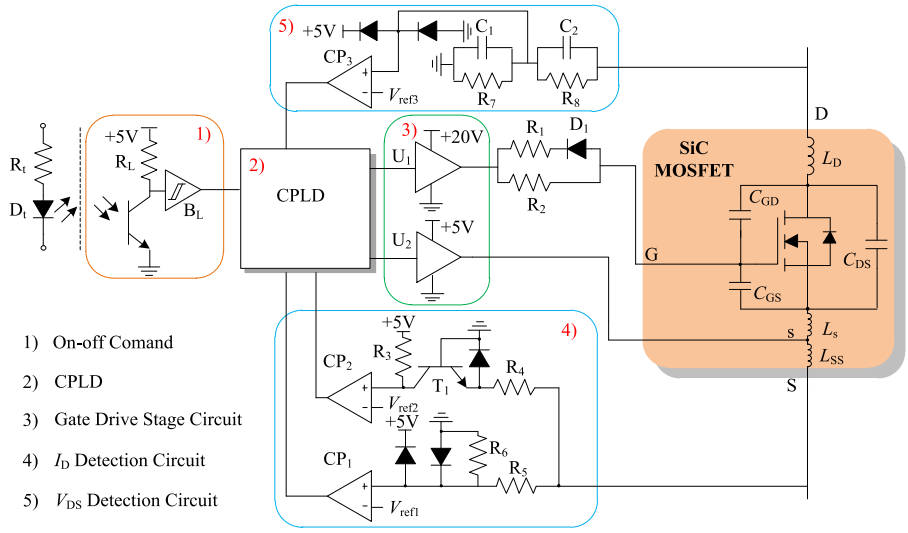


Fig. 6. Detailed circuit implementation of the proposed AGD.

nize the switching intervals of the SiC MOSFET, which provide a reliable basis for delay time (t_{d1} and t_{d2}) calculations. In addition, it is important to mention that all the comparators used in this design are high-speed devices due to a low-voltage (+5 V) power supply.

C. Consideration for Optimal Delay Time t_{d1} and t_{d2}

As mentioned earlier, t_{d1} and t_{d2} are the key parameters that influence the behavior of the I_D and $V_{\rm DS}$. In order to achieve an optimal design, the value of the t_{d1} and t_{d2} should be carefully selected to pursue a tradeoff between switching losses and switching stress.

The switching losses calculations are based on the typical waveforms of I_D and $V_{\rm DS}$, which are shown in Fig. 4 for turn-ON and in Fig. 5 for turn-OFF, respectively. Piecewise linear current and voltage slopes are assumed to simplify the calculation. The total energy losses at turn-ON transient are mainly generated by current rise, voltage decay, and the reverse recovery effect. In addition, the energy losses during turn-OFF can be calculated as the sum of the losses induced by voltage rise and current decay. Therefore, the switching losses in both condition can be expressed as

$$E_{\rm ON} = E_{{\rm on},dI_D/dt} + E_{{\rm on},dV_{\rm DS}/dt} + E_{I{\rm rr}} \tag{8}$$

$$E_{\rm OFF} = E_{{\rm off},dV_{\rm DS}/dt} + E_{{\rm off},dI_D/dt}. \tag{9}$$

At turn-ON transient, the energy losses during the current rise and the voltage decay can be expressed as

$$E_{{\rm on},dI_D/dt} = \frac{1}{2}\cdot I_L\cdot(V_{\rm DC} - L_{\rm loop}\cdot|dI_D/dt|)\cdot\frac{I_L}{|dI_D/dt|} \tag{10}$$

$$E_{{\rm on},dV_{\rm DS}/dt} = \frac{I_L\cdot V_{\rm DC}}{2}\cdot\frac{V_{\rm DC}}{|dV_{\rm DS}/dt|}\cdot(1-\sigma)^2 \tag{11}$$

where $L_{\rm loop}$ is the stray inductance in the power loop and

$$\sigma = \frac{V_{\rm OS}}{V_{\rm DC}} = \frac{L_{\rm loop}\cdot|dI_D/dt|}{V_{\rm DC}}. \tag{12}$$

On the other hand, expressions to characterize the peak current and the energy loss generated by the reverse recovery effect were given in [36], as presented in the following:

$$I_{\rm rr} = \sqrt{Q_{\rm rr}\cdot|dI_D/dt|} \tag{13}$$

$$E_{I{\rm rr}} = \left(I_L\cdot\sqrt{\frac{Q_{\rm rr}}{|dI_D/dt|}} + Q_{\rm rr}\right)\cdot V_{\rm DC}\cdot(1-\sigma) \tag{14}$$

where $Q_{\rm rr}$ is the reverse recovery charge.

Therefore, according to (7), (9), (10), and (12), the energy loss during the turn-ON transient can be expressed as the following equation:

$$E_{\rm ON} = \underbrace{\frac{I_L\cdot V_{\rm DC}}{2}\cdot\left(\frac{I_L}{|dI_D/dt|} + \frac{V_{\rm DC}}{|dV_{\rm DS}/dt|}\cdot(1-\sigma_S)^2\right)}_{\text{Loss due to limited rates of } I_D \text{ and } V_{\rm DS} \text{ change}} + \underbrace{\left(I_L\cdot\sqrt{\frac{Q_{\rm rr}}{|dI_D/dt|}} + Q_{\rm rr}\right)\cdot V_{\rm DC}\cdot(1-\sigma_S)}_{\text{Loss due to reverse recovery effect}} - \underbrace{\frac{1}{2}\cdot L_S\cdot I_{\rm Loop}{}^2}_{\text{Energy to } L_S}. \tag{15}$$

Similarly, the energy loss at turn-OFF transient can be expressed as

$$E_{\rm OFF} = \underbrace{\frac{I_L\cdot V_{\rm DC}}{2}\cdot\left(\frac{I_L}{|dI_D/dt|} + \frac{V_{DC}}{|dV_{\rm DS}/dt|}\cdot(1+\sigma_S)^2\right)}_{\text{Loss due to limited rates of } I_D \text{ and } V_{\rm DS} \text{ change}} + \underbrace{\frac{1}{2}\cdot L_S\cdot I_{\rm Loop}{}^2}_{\text{Energy from } L_S}. \tag{16}$$

Accordingly, the switching energy losses in applications can be calculated with the value of $dV_{\rm DS}/dt$ and dI_D/dt. However, the value of $dV_{\rm DS}/dt$ and dI_D/dt in the proposed AGD method is not a constant due to the different gate drive voltage applied. In addition, the loss generated by changed voltage slope is not obvious due to the high value of $dV_{\rm DS}/dt$ in SiC MOSFET. In order to further simplify the calculation only the current slope

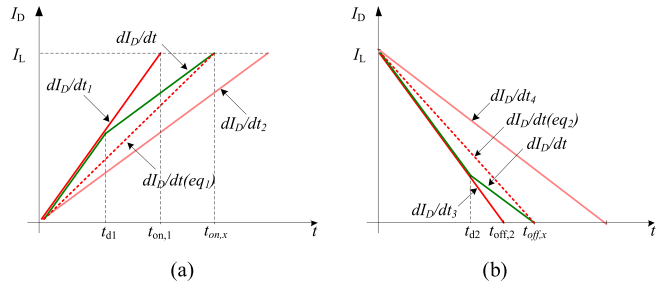


Fig. 7. Schematic diagram of the equivalent current slope. (a) Turn-ON. (b) Turn-OFF.

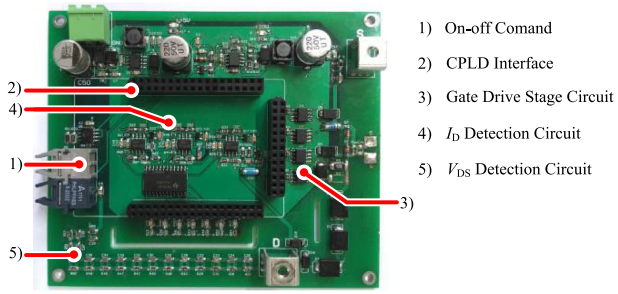


Fig. 8. Hardware prototype of the AGD

changing is taken into consideration, and the changing current slope is equivalent to a constant current slope according to the principle of equal current (e.g., I_L) at the same time as shown in Fig. 7.

In Fig. 7, dI_D/dt_1 and dI_D/dt_2 are the value of the current slope under the V_{GG} of 20 and 15 V, respectively. dI_D/dt_3 and dI_D/dt_4 represent the value of the current slope under the V_{GG} of –5 and 0 V. In addition, $t_{on,1}$ and $t_{on,2}$ are the rising time under the dI_D/dt_1 and dI_D/dt_3, respectively. Therefore, $t_{d1} \in [0, t_{on,1}]$ and $t_d \in [0, t_{off,2}]$. Moreover, dI_D/dt represents the actual current slope, $dI_D/dt_{(eq1)}$ and $dI_D/dt_{(eq2)}$ represent the equivalent current slope at turn-ON and turn-OFF, respectively. $t_{on,x}$ and $t_{off,x}$ are the equivalent time of the current rising/falling. According to the principle of the equal current, the following equation can be obtained:

$$\begin{aligned} I_L &= |dI_D/dt_1| \cdot t_{d1} + |dI_D/dt_2| \cdot (t_{on,x} - t_{d1}) \\ &= \left|dI_D/dt_{(eq1)}\right| \cdot t_{on,x} \end{aligned} \tag{17}$$

and the equivalent rising time $t_{on,x}$ of the current can be expressed as

$$t_{on,x} = \frac{I_L - (|dI_D/dt_1| - |dI_D/dt_2|) \cdot t_{d1}}{|dI_D/dt_2|}. \tag{18}$$

Thus, the value of the equivalent current slope at turn-ON can be expressed as

$$\left|dI_D/dt_{(eq1)}\right| = \frac{I_L \cdot |dI_D/dt_2|}{I_L - (|dI_D/dt_1| - |dI_D/dt_2|) \cdot t_{d1}}. \tag{19}$$

Similarly, the value of the equivalent current slope at turn-OFF can be expressed as

$$\left|dI_D/dt_{(eq2)}\right| = \frac{I_L \cdot |dI_D/dt_4|}{I_L - (|dI_D/dt_3| - |dI_D/dt_4|) \cdot t_{d2}}. \tag{20}$$

It can be seen from (19) and (20) that with the increment of the delay time, the equivalent current slope will increase. As a consequence, the energy losses will be reduced and the I_{rr} and V_{OS} will be increased.

According to (1)–(4), (13), (15), and (19), the E_{ON} and I_{rr} can be expressed as a function of the variable t_{d1}. Similarly, the E_{OFF} and V_{OS} can be expressed as a function of the variable t_{d2} according to (1)–(4), (12), (16), and (20). Moreover, the delay time t_{d1} and t_{d2} reach the optimal values when (21) and (22) are fulfilled

$$\frac{|E_{ON}(t_{d1}) - E_{ON}(0)|}{|E_{ON}(t_{on,1}) - E_{ON}(0)|} = \frac{|I_{rr}(t_{d1}) - I_{rr}(0)|}{|I_{rr}(t_{on,1}) - I_{rr}(0)|} \tag{21}$$

$$\frac{|E_{OFF}(t_{d2}) - E_{OFF}(0)|}{|E_{OFF}(t_{off,2}) - E_{OFF}(0)|} = \frac{|V_{OS}(t_{d1}) - V_{OS}(0)|}{|V_{OS}(t_{off,2}) - V_{OS}(0)|}. \tag{22}$$

D. Hardware Prototype

In Fig. 8, a prototype of the AGD was developed which mainly contains five parts as shown in Fig. 6. In addition, an external CLPD core board running at 200 MHz will be connected to the AGD through the CLPD interface.

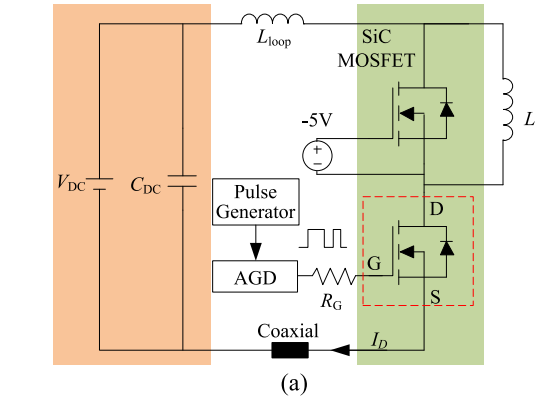
IV. Experimental Verification

In order to evaluate the performance of the proposed AGD, the double pulse test is carried out as shown in Fig. 9. In Fig. 9(a), the power devices used in test are 1.2 kV/300 A SiC MOSFET modules (CAS300M12BM2) from CREE. The lower SiC MOSFET serves as the device under test and the upper one serves as the freewheeling diode. A film capacitor acts as the dc bus support capacitor and an air-core inductor L serves as inductive load. Fig. 9(b) shows the photographs of the experimental setup. The corresponding parameters of the tested module are presented in Table I. The parasitic capacitances were extracted from the datasheet and the parasitic inductances were measured in combination with the existing method presented in [37]. In addition, the detailed parameters of test bench and measurement equipment used in the test are presented in Table II.

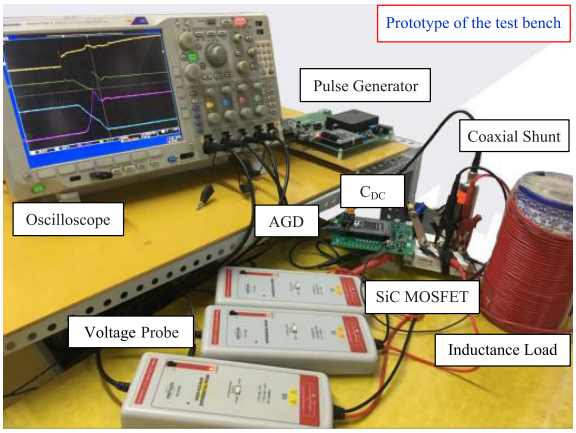
A. Experimental Verification of the Proposed AGD

In order to verify the feasibility of the proposed AGD, in this section, experimental verification is carried out with the gate resistance 10 Ω both in turn-ON and turn-OFF, the dc bus voltage is 500 V and the switched current is 280 A. The optimized delay time t_{d1} of 70 ns and t_{d2} of 110 ns were calculated by (21) and (22). In addition, a propagation time of about 34 ns caused by the AGD has been taken into consideration in the experiments. Fig. 10 shows the experimental waveforms for SiC MOSFET with the proposed AGD.

It can be seen that when the turn-ON signal arrives as shown in Fig. 10(a), the high V_{GG} (i.e., 20 V) is applied to the gate terminal first. As soon as the I_D starts to rise, the negative voltage V_{SS} is detected by controller. After the delay time t_{d1},



(a)



(b)

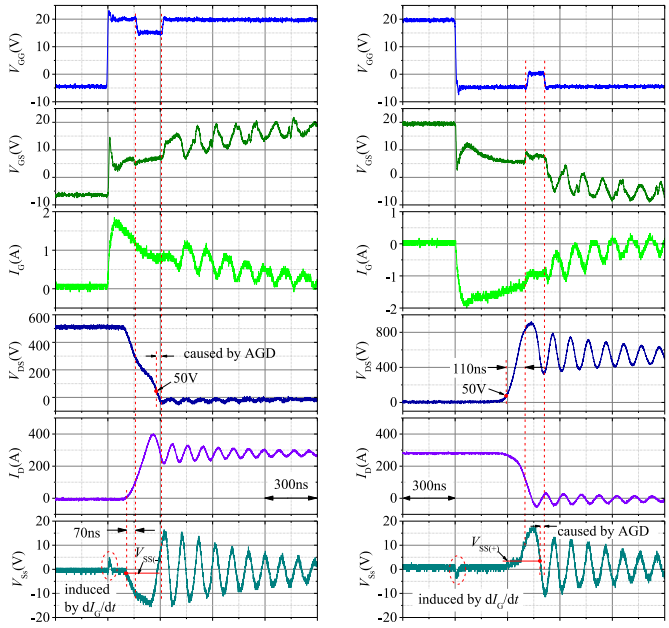
Fig. 9. Experimental setup. (a) Circuit diagram. (b) Photograph.

TABLE I
PARAMETERS FOR CALCULATIONS OF THE ENERGY LOSSES AND OVERSHOOTS

Parameters	V_{TH}	g_m	C_{iss}	C_{GD}	Q_{rr}	L_s	L_{SS}
Value	2.5 V	156 S	19.3 nF	0.12 nF	1.2 μC	3.6 nH	3.6 nH

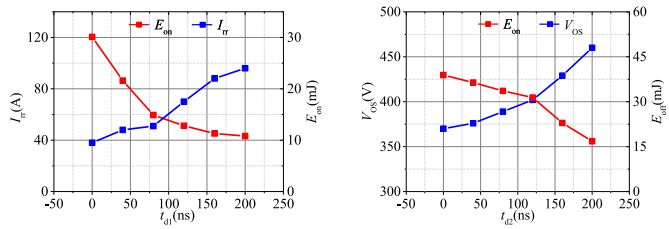
TABLE II
INFORMATION OF MEASUREMENT EQUIPMENT AND TEST BENCH

Name	Information
Oscilloscope	Tektronix MDO4104-3, 3 GHz, 5 GS/s
V_{DS}	Pintech N1050B, Probe 1:100, 1.5 kV/100 MHz
V_{GS}, V_{SS}	Pintech N1050B, Probe 1:50, 150 V/100 MHz
I_G	Tektronix, TCP0030A, 30 A/120 MHz
I_D	Coaxial shunt, 0.02Ω SSDN-02, 2 kA/800 MHz
C_{DC}	1020 μF/1.1 kV
L	300 μH
L_{loop}	140.5 nH



(a) (b)

Fig. 10. Experimental waveforms for SiC MOSFET with the proposed AGD. (a) Turn-ON with $t_{d1} = 70$ ns and $R_{on} = 10\ \Omega$. (b) Turn-OFF with $t_{d2} = 110$ ns and $R_{off} = 10\ \Omega$.



(a) (b)

Fig. 11. Effect of delay time on overshoots and switching energy losses. (a) Turn-ON. (b) Turn-OFF.

which is 70 ns as calculated, the V_{GG} is reduced to 15 V, and the gate voltage V_{GS} and current I_G both decrease significantly. When the V_{DS} drops to below the 10% of V_{DC} (i.e., 50 V), the high V_{GG} is restarted to charge the SiC MOSFET.

At turn-OFF transient, the SiC MOSFET is first discharged by the negative V_{GG} (i.e., -5 V) as shown in Fig. 10(b). When the V_{DS} starts to rise above 50 V, comparator circuit sends the signal to the controller. After the delay time t_{d2} of 110 ns, the V_{GG} becomes 0 V and the V_{GS} and I_G have risen obviously. Subsequently, when the I_D drops to zero, the positive V_{SS} is detected because it drops below the $V_{SS(+)}$ and the negative V_{GG} is reactivated to provide a reliable turn-OFF for the SiC MOSFET.

It is worth noting that the dI_D/dt and dI_G/dt induced voltage across the L_{SS} which appear at different stages can be easily identified due to its different orientation.

As mentioned earlier, the delay time t_{d1} and t_{d2} are the key parameters that influence the switching behavior of SiC MOSFET. In order to demonstrate the relationship between delay time and switching characteristics, more experiments have been carried out and the experiment results are shown in Fig. 11. Since the time of current and voltage slope is about 200 ns both at turn-ON and turn-OFF transient, the delay time t_{d1} and t_{d2} are increased from 0 to 200 ns to show the differences, respectively.

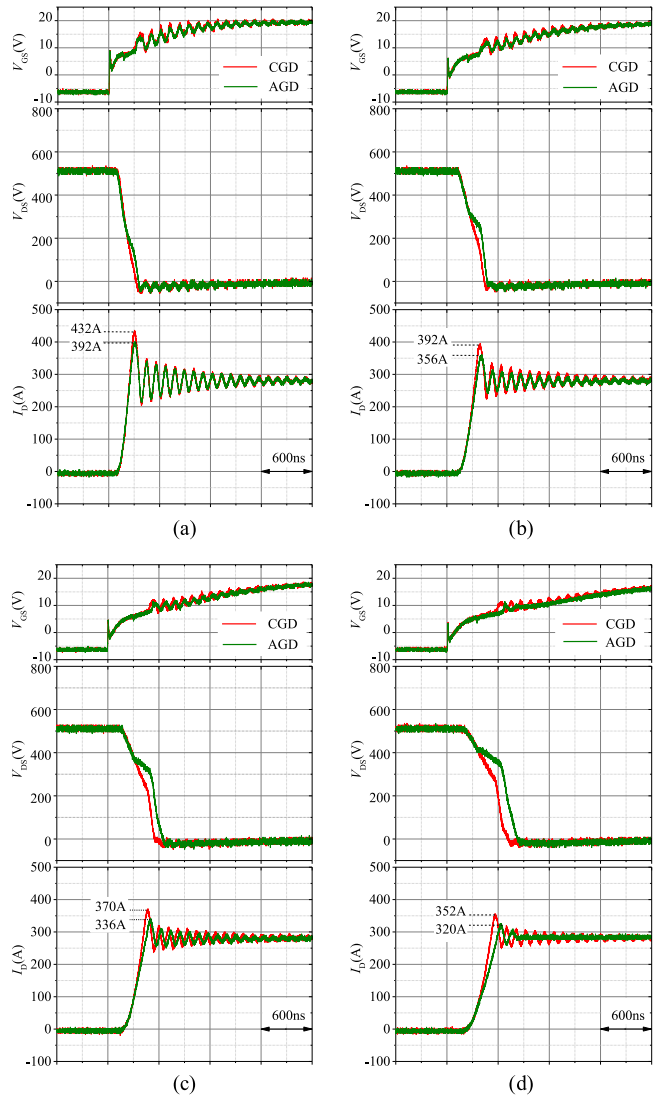


Fig. 12. Turn-ON performance comparison of SiC MOSFET between AGD and CGD. (a) $R_{\rm on} = 5\ \Omega$ with $t_{d1} = 50$ ns. (b) $R_{\rm on} = 10\ \Omega$ with $t_{d1} = 70$ ns. (c) $R_{\rm on} = 15\ \Omega$ with $t_{d1} = 100$ ns. (d) $R_{\rm on} = 20\ \Omega$ with $t_{d1} = 130$ ns.

It can be seen that with the increase of the delay time, the energy losses are reduced and the overshoots are increased in both conditions. However, when td1 of about 70 ns during turn-ON and t_{d2} of about 110 ns during turn-OFF is applied respectively, a tradeoff between the energy losses and the overshoots can be achieved relatively.

B. Comparison to Conventional Gate Driver (CGD)

In order to demonstrate the advantages of the AGD in both the overshoots and oscillations compared to CGD, more experiments were carried out under different gate resistances, operation temperatures, and load currents. The detailed experimental comparisons between these two methods are presented as follows.

1) Turn-ON Performance Comparison: Fig. 12 shows the turn-ON performance comparisons of SiC MOSFET between CGD and AGD under different gate resistances. In Fig. 12, the dc bus voltage is 500 V, the switched load current is 280 A, and the gate resistance in both gate drivers are increased from 5 to 20 Ω (with a resolution of 5 Ω) to show the differences. It can be seen that the overshoots of the I_D in AGD are lower than those in CGD with fixed drive voltage at various gate resistances. In addition, the oscillation amplitude of the $V_{\rm GS}$, current I_D, and voltage $V_{\rm DS}$ in the AGD is smaller than those in CGD under the same gate resistance. Especially with the increase of the gate resistance, the oscillations are damped obviously.

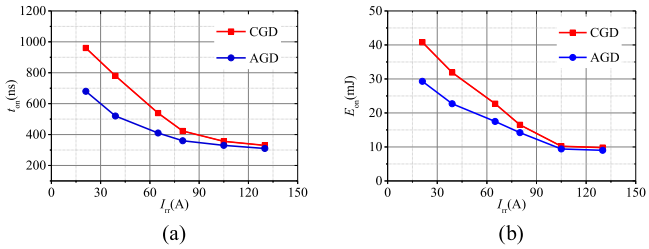


Fig. 13. Turn-ON switching performance comparison between AGD and the CGD under same current overshoot. (a) Turn-ON time. (b) Turn-ON energy losses.

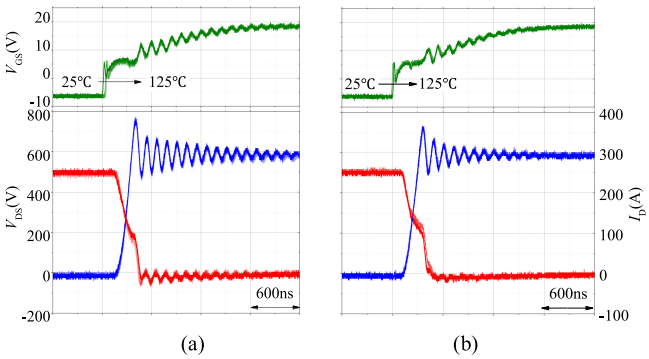


Fig. 14. Turn-ON performance comparison of SiC MOSFET between CGD and AGD under different operation temperatures. (a) CGD. (b) AGD.

In order to further demonstrate the advantages of the proposed AGD method, Fig. 13 shows the turn-ON energy losses and turn-ON time comparisons between AGD and the CGD at same current peaks. The gate resistance $R_{\rm on}$ of the CGD method and the delay time $t_{\rm d1}$ are changed to obtain various current peaks. Obviously, the energy losses and turn-ON time of the proposed AGD are always lower than those in CGD method. In CGD, to achieve the smaller current peak, the larger gate resistance is utilized, which results in more turn-ON energy loss and turn-ON time. Especially, when a current overshoot of 21 A is achieved by both methods, a 28% energy loss reduction and a 29% turn-ON time reduction are obtained by the proposed AGD.

More tested waveforms comparison of SiC MOSFET between CGD and AGD under different operation temperatures and load currents are shown in Figs. 14 and 15.

In the experiment of the different operation temperatures, the dc bus voltage is 500 V, the switched load current is 280 A, the gate drive resistance $R_{\rm on}$ is 10 Ω, and the optimal delay time t_{d1} is 70 ns. All these parameters are consistent with 25 °C. It can be seen from Fig. 14 that the impact of the operation temperature on the voltage and current slopes is limited since the performance

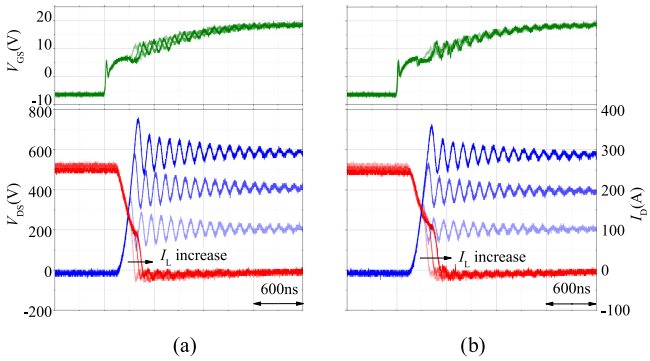


Fig. 15. Turn-ON performance comparison of SiC MOSFET between CGD and AGD under different load currents. (a) CGD. (b) AGD.

of the SiC MOSFETs varies little with different operation temperature, only the turn-ON delay time changed obviously. the higher the operation temperature, the lower the turn-ON delay time. However, the performance of the AGD will not be affected by the changes in turn-ON delay time since the detection circuits can detect the voltage and current stages accurately. Therefore, the AGD can provide an optimal performance under different operation temperatures. It is worth mentioning that the overshoots of the I_D in AGD are always lower than those in CGD. In addition, the oscillation amplitudes of the $V_{\rm GS}$, I_D, and $V_{\rm DS}$ in the AGD are smaller than those in CGD.

In the experiment of the different load currents, the dc bus voltage is 500 V, the gate drive resistance $R_{\rm on}$ is 10 Ω, and the optimal delay time t_{d1} is 70 ns. The switched load current for two gate drivers are both increased from 100 to 300 A to show the differences. It can be observed from Fig. 15 that the turn-ON delay times and the current slopes maintain nearly constant as the load current increases. Besides, the turn-ON voltage falling rate decreases as the load current rises, but it is not obvious as shown in the Fig. 15. In addition, the overshoots of the I_D in AGD are always lower than those in the CGD and the oscillation amplitudes of the $V_{\rm GS}$, I_D, and $V_{\rm DS}$ in the AGD are smaller than those in CGD under different load currents.

It should be pointed out that the optimal delay time is impacted by the changes of the load current according to (21) and (22). With the delay time of 70 ns, the smaller the load current, the greater the deviation of optimal parameters. However, the smaller the load current switched, the lower the switching losses and overshoots. Therefore, the deviation of optimal parameters induced by the load current changes can be neglected.

2) Turn-off Performance Comparison: As shown in Fig. 16, the turn-OFF performance comparison of SiC MOSFET between CGD and AGD with different gate resistances (5 to 20 Ω) is also conducted under a dc bus 500 V and load current of 280 A. It can be seen that the overshoots of voltage $V_{\rm DS}$ in AGD are always lower than those in CGD. In addition, the oscillation amplitude of the $V_{\rm GS}$, I_D, and $V_{\rm DS}$ in the AGD are smaller than those in CGD under the same gate resistance. Especially with the increase of the gate resistance, the oscillations are damped obviously.

The turn-OFF energy losses and turn-OFF time comparisons for both gate drive methods at same voltage overshoot are shown

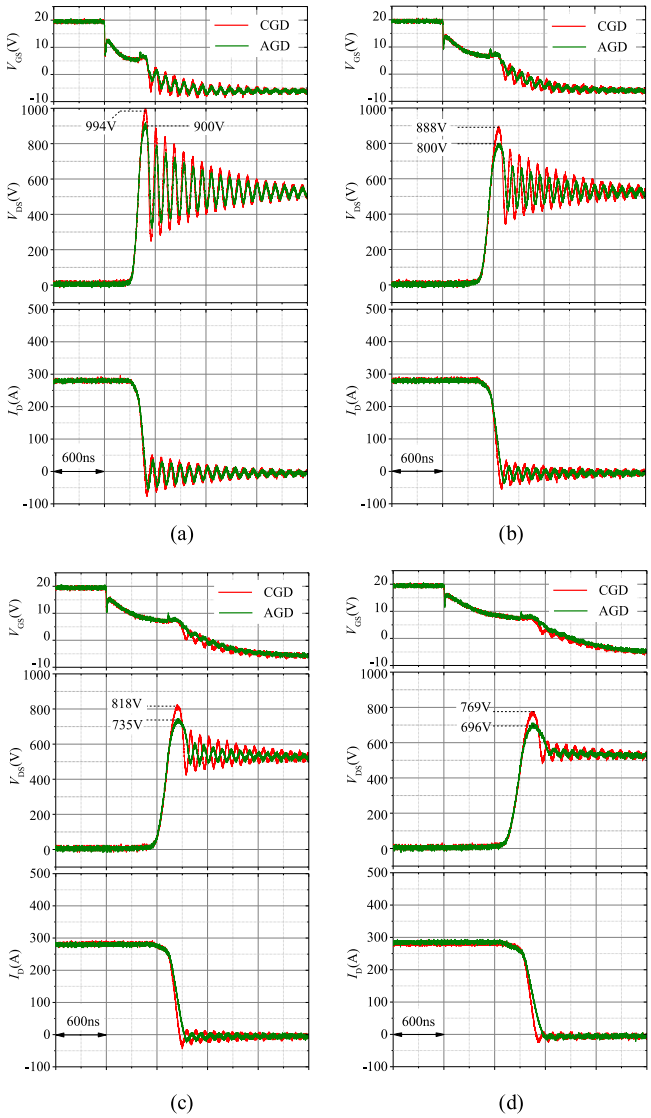


Fig. 16. Turn-OFF performance comparison of SiC MOSFET between AGD and CGD. (a) $R_{\rm off} = 5\ \Omega$ with $t_{d2} = 80$ ns. (b) $R_{\rm off} = 10\ \Omega$ with $t_{d2} = 100$ ns. (c) $R_{\rm off} = 15\ \Omega$ with $t_{d2} = 150$ ns. (d) $R_{\rm off} = 20\ \Omega$ with $t_{d2} = 180$ ns.

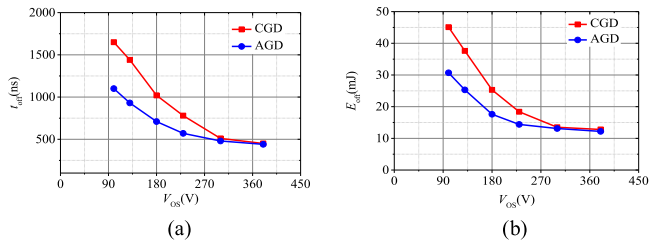


Fig. 17. Turn-OFF switching performance comparison between AGD and the CGD under same voltage overshoot. (a) Turn-OFF time. (b) Turn-OFF energy losses.

in Fig. 17. The gate resistance $R_{\rm off}$ of the CGD method and the delay time t_{d2} are controlled to achieve various voltage spikes. It shows that the turn-OFF energy losses and turn-OFF time are increasing with the decrease of overvoltage amplitude. When $V_{\rm OS}$ reaches a high value of 380 V, the turn-OFF losses and turn-OFF time of the SiC MOSFET with both method are similar due to

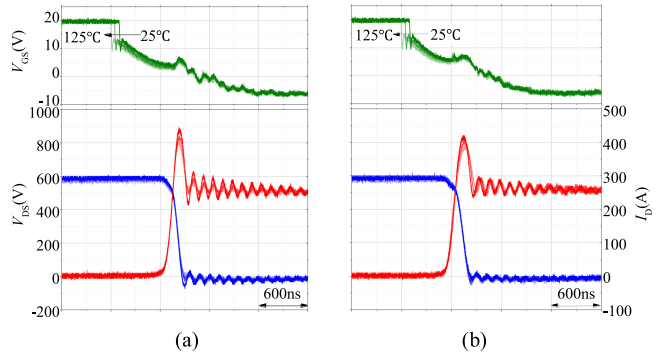


Fig. 18. Turn-OFF performance comparison of SiC MOSFET between CGD and AGD under different operation temperatures. (a) CGD. (b) AGD.

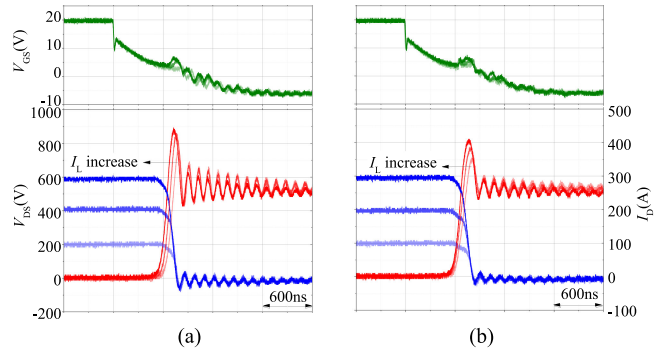


Fig. 19. Turn-OFF performance comparison of SiC MOSFET between CGD and AGD with different load currents. (a) CGD. (b) AGD.

similar switching speed. When $V_{\rm OS}$ is applied with a low value of 100 V, the turn-OFF losses and turn-OFF time of the proposed AGD are 32% and 33% of that in CGD, respectively.

The turn-OFF performance comparison of SiC MOSFET under different operation temperatures and load currents amplitude are also shown in Figs. 18 and 19, respectively. The dc bus voltage and gate resistance are fixed at 500 V and 10 Ω, respectively. The optimal delay time t_{d2} maintains 110 ns. In the different temperatures tests, the turn-OFF delay times increases as the operation temperature rises, while the voltage and current slopes maintain almost constant as shown in Fig. 18. Similar to the turn-ON transient, only the turn-OFF delay time obviously changed under different operation temperatures.

Thus, the AGD can also provide an optimal performance at turn-OFF transient.

In the different load current tests, the turn-OFF delay times decreases as the load current rises. The voltage and current slopes changes are not obvious, as shown in Fig. 19. With the delay time of 110 ns, the smaller the load current, the greater the deviation of optimal parameters. Similar to turn-ON transient, this deviation also can be neglected.

In both cases, with the AGD applied, the overshoots of the $V_{\rm DS}$ in AGD are always lower than those in CGD and the oscillation amplitudes of all the signals in AGD are obviously lower compared to CGD.

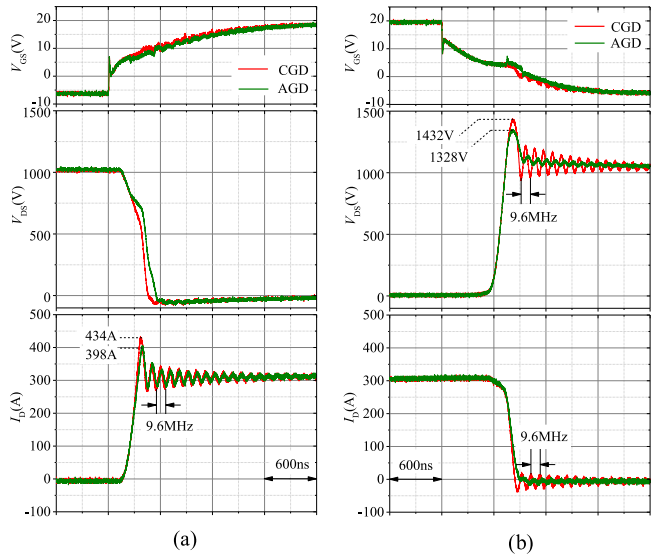


Fig. 20. Switching performance comparison of SiC MOSFET (1.7 kV/300 A) between CGD and AGD. (a) Turn-ON with $R_{\rm on} = 10\ \Omega$, $t_{d1} = 150$ ns. (b) Turn-OFF with $R_{\rm off} = 10\ \Omega$, $t_{d2} = 220$ ns.

C. Using in Different SiC MOSFETS

In order to further verify the feasibility of the proposed AGD, experiments are carried out with another SiC MOSFETs (1.7 kV/300 A) modules from CREE and the experimental results are shown in Fig. 20. In Fig. 20, the dc bus voltage is 1 kV and the switched load current is 280 A. By using the CGD with fixed drive voltage, the current and voltage oscillations are obviously with resonant frequency at 9.6 MHz and maximum $V_{\rm DS}$ and I_D amplitude of 1432 V and 434 A occur, respectively. However, the AGD not only reduces the current and voltage overshoot, but also suppresses the voltage oscillations significantly.

Based on the aforementioned experiments, it can be concluded that there are two parameters of the AGD that need to be set in the application of a SiC MOSFET: detection thresholds and optimal delay time. According to (5)–(7), the detection thresholds are determined by the dc bus voltage and the parasitic inductance $L_{\rm SS}$ of the SiC MOSFET module. In addition, the optimal delay time is mainly determined by parameters of the SiC MOSFET module, gate drive resistance, and load current according to the (1)–(4), (21), and (22). However, the impact of the load current is limited; therefore, the detection thresholds and optimal delay time of the AGD only need to be set once when the dc bus voltage and gate drive resistance are confirmed in the application of an SiC MOSFET, whether using in one device or two legs.

V. Analysis and Discussion

A. Electromagnetic Interference Analysis

As shown in Figs. 12 and 16, the proposed AGD has the capability of suppressing the overshoots and oscillations in $V_{\rm DS}$ and I_D. In general, the high dV/dt induced by high switching speed is the key factor conduced EMI production in power

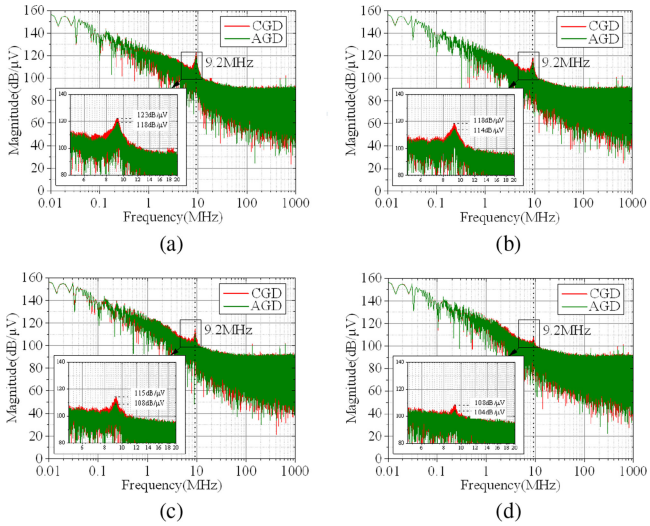


Fig. 21. Spectrum comparison between CGD and AGD for $V_{\rm DS}$ experimental results. (a) $R_{\rm G} = 5\,\Omega$. (b) $R_{\rm G} = 10\,\Omega$. (c) $R_{\rm G} = 15\,\Omega$. (d) $R_{\rm G} = 20\,\Omega$.

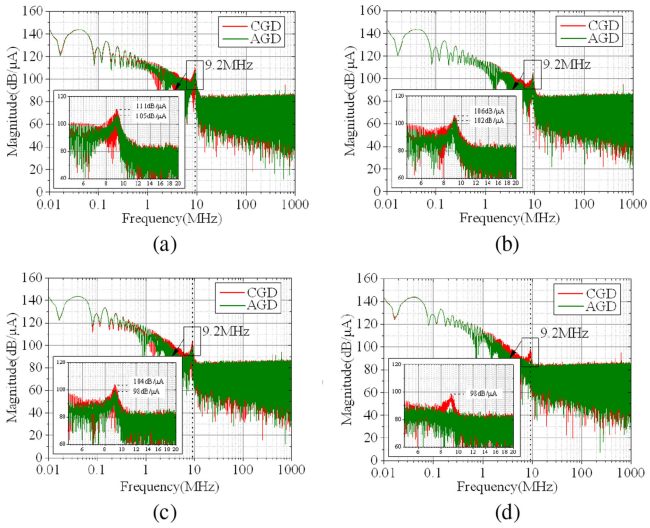


Fig. 22. Spectrum comparison between CGD and AGD for I_D experimental results. (a) $R_G = 5\,\Omega$. (b) $R_G = 10\,\Omega$. (c) $R_G = 15\,\Omega$. (d) $R_G = 20\,\Omega$.

electronic equipment. In order to have an understanding of the EMI induced by high *dI*/*dt* and *dV*/*dt*, EMI analysis including the oscillation in the voltage and current waveforms are carried out, respectively. Accordingly, the effect of oscillations can be characterized considering the current or voltage source as a periodic trapezoidal pulse and fast Fourier transform (FFT) analysis.

The approximation of the spectrum for both $V_{\rm DS}$ and I_D are shown in Figs. 21 and 22. These data were obtained by the oscilloscope Tektronix MDO4104-3 in experiment and the spectrum was obtained applying the FFT in MATLAB software after the data were processed. The results show that the AGD can reduce the EMI generation effectively from 1 to 10 MHz in $V_{\rm DS}$ and I_D. Especially, the AGD eliminates the noise in $V_{\rm DS}$ and I_D with resonant frequency of 9.2 MHz at $R_G = 20\,\Omega$. It should be mentioned that the $V_{\rm DS}$ and I_D measures were in common mode conditions.

B. Cost Analysis

As mentioned earlier, the AGD not only can drive the SiC MOSFET but also can optimize its switching performance. In high power applications with the CGD, however, the snubber circuits are indispensable to suppress the overvoltage and EMI problems in order to obtain a better performance. With the increase of the system capacity, on the other hand, the greater the volume of the snubber circuits are required, the lower the system efficiency are induced.

According to Fig. 8, in order to successfully implement the AGD, two MOSFET gate drivers IXDN609SIA with the price $2.2 per unit from IXYS Integrated Circuits and three high-speed comparators AD8611ARMZ-R2 with the price $6.1 per unit from Analog Devices were used. In addition, a controller (CPLD Lattice LC42182ZE-7TN100C) core board was used with the price $6.6 per unit. In the design of the proposed AGD, the cost is mainly from aforementioned three parts. It is estimated that the cost is approximate $10 for the rest of the components and for each isolated dc/dc power supply is about $10; therefore, the total cost of the AGD for dual-channel is about $98.6 and it was calculated just for a few, not for large series. However, the cost of the CGD plus snubber circuits is far more than that in AGD. For example, the gate driver PT62SCMD17 from CREE for high power SiC MOSFETs is priced at $144. On the other hand, the cost of snubber circuits for high power applications is more. For instance, an inverter module used in the 100 kW locomotive auxiliary converter application, which employed 1700 V/300 A SiC MOSFETs, needs one gate driver and one snubber capacitance in one bridge leg in general. The cost of the gate driver PT62SCMD17 and the snubber capacitance MKP386M468200JT3 (Vishay) is about $160. Therefore, the use of the AGD not only saves the cost but also improves the power density of the inverter module.

VI. Conclusion

In this paper, a novel AGD with multi-voltage for improving switching performance of high power SiC MOSFETs is presented under hard switching conditions. In addition, the optimal drive voltage switching delay time has been analyzed and calculated considering a tradeoff between switching losses and switching stress. With the optimized delay time t_{d1} and t_{d2}, the AGD can effectively minimize the overshoots and suppress the oscillations. The performance of the proposed AGD was verified in double pulse test under different operation temperatures and load currents and the results show that the AGD can reduce the current peak at turn-ON and minimize the overvoltage at turn-OFF. On the other hand, the proposed AGD can not only suppress the oscillation of the voltage but also attenuate the oscillation of the current induced by high switching speed and parasitic elements from 1 to 10 MHz in this paper. In addition, the AGD was validated by another SiC MOSFET and the results demonstrate that the AGD can be applied in different SiC MOSFETs successfully. Although the AGD requires two driver ICs, three high-speed comparators and a controller, it is a good solution due to its implement simplicity and low cost. In addition, no negative drive voltage in AGD is required compared

to the CGD. In the high power applications, therefore, the proposed AGD has more advantage in cost and efficiency compared to conventional method with CGD and snubber circuits.

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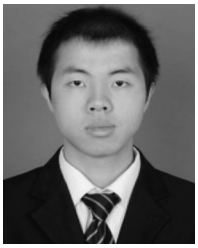

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