LETTER

A high voltage diode with partial n⁺ adjusting region embedded at the anode side

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Abstract A novel high voltage diode featuring partial n⁺ adjusting region embedded at the anode side is proposed and analyzed by device simulation in this paper. The low and inverted on-state carrier profile is obtained to realize the fast and soft recovery behavior. The simulations show that the proposed diode achieves a 21% reduction in the reverse peak current density compared with the conventional diode. What's more, such partial n⁺ adjusting region results in the parasitic npn transistor triggered during reverse recovery, and electrons are injected into the pn⁻ junction to inhibit the peak electric field, improving the dynamic ruggedness.

Keywords: dynamic avalanche, current filament, high voltage diode, reverse recovery

Classification: Power devices and circuits

1. Introduction

Great challenge for the high voltage diode above 3.3 kV in the IGBT application is to ensure the fast and soft recovery behavior, especially the dynamic avalanche capability under extreme over-stress operating condition [1, 2]. Such high di/dt, high parasitic inductance L and high supply voltage V_{dc} can provoke the appearance of dynamic avalanche, leading to the diode destruction [3, 4, 5, 6, 7]. In previous work, the $p^+pn^-nn^+$ structure has been proposed to improve the reverse recovery behavior [8, 9]. The conventional anode structure, however, is limited to improve the fast and soft recovery behavior, because of the larger carrier concentration at the anode side than at the cathode side for the uniform carrier lifetime [3, 10, 11]. In addition, the carrier lifetime technologies, for instance electron or proton irradiation [12, 13, 14, 15, 16], were introduced to provide a low plasma density in front of p^+ emitter to improve the fast and soft recovery behavior. Some new cathode structures including the Field Charge Extraction (FCE) cathode [17, 18, 19] and the Controlled Injection of Backside Holes (CIBH) structure [20, 21] were also proposed to improve the dynamic ruggedness. Nevertheless, these cathode structures are only to suppress the second electric field peak at the cathode side by injecting the holes into the n^-n junction [11, 18, 22], while leading to an unexpected increase in the reverse peak current density (J_{RM}), hence the power loss increases as well.

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In this paper, a novel high voltage diode with the n⁺ adjusting region at the anode side is proposed, and the mechanisms that the npn transistor is triggered and the electric field is modulated by electrons during reverse recovery are studied and simulated. This structure realizes the improved fast recovery behavior and the dynamic avalanche capacity compared with the conventional diode.

2. Device structures and operating mechanism

Fig. 1(a) and (b) show the structure schematics of the conventional diode (CD) and the proposed n⁺ adjusting region diode (NARD), respectively. Two diodes have the same n⁻ base, the same p buffer layer at the anode side, and the same n⁺ emitter and n buffer layer at the cathode side.
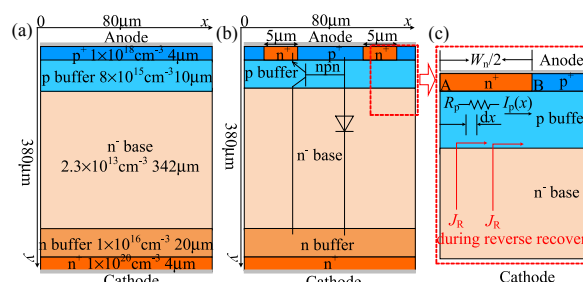

Fig. 1. Structure schematics: (a) the conventional diode (CD), (b) proposed n⁺ adjusting region diode (NARD). (c) Local current flow of the anode side during reverse recovery in the NARD.

The n⁻ base doping is $N_D = 2.3 \times 10^{13}$ cm⁻³ and realizes a blocking capability of 3.3 kV. The p and n buffer layers are both the Gaussian doping profiles, and the corresponding surface doping concentrations are 8×10^{15} cm⁻³ and 1.0×10^{16} cm⁻³, respectively. However, the only difference is that the highly doped n⁺ adjusting region with a surface doping concentration of 1.0×10^{20} cm⁻³ are embedded in the p⁺ emitter in the NARD, and the width of the n⁺ adjusting region (W_n) is 5.2 μm.

During reverse recovery, the NARD structure is equivalent to a conventional diode in parallel with an npn transistor, in which the n⁺ adjusting region of the anode side acts as the emitter, and the p buffer layer acts as the base, and the n⁻ base of the diode represents the collector, as shown in Fig. 1(b). The local current flow of the anode side during reverse recovery in the NARD is illustrated in Fig. 1(c). At the initial stage of reverse recovery, the holes extracted from the n⁻ base flow laterally across the p buffer layer underneath the n⁺ adjusting region of the anode side.

As a result, the current $I_p(x)$ flows through the p$^+$ emitter, leading to the voltage drop $V_p(t)$ across the resistance (R_p) of the p buffer layer. With the increase of reverse current density, when the reverse voltage $V_p(t)$ is equal to V_{bi} about 0.7 V, the parasitic npn transistor is triggered, and electrons of the n$^+$ adjusting region start to inject into the p buffer layer.

The condition for the forward biasing of the pn$^+$ junction at the anode side during reverse recovery can be derived by two dimensional analysis. From the Fig. 1(c), the reverse current flows through the p buffer layer from the middle of the n$^+$ adjusting region (at point A) to the p$^+$ emitter (at point B). The current flowing through a variation part (dx) in the p buffer layer along the anode side direction is expressed by dI_p. Therefore, the reverse current flowing through the p buffer layer from the middle of the n$^+$ adjusting region (at point A) to x is given by

$$I_p(x) = \int_0^x dI_p = \int_0^x J_R L dx = J_R L x \tag{1}$$

where L is the length of the n$^+$ adjusting region perpendicular to the cross section of two dimension. The p buffer resistance of the dx thickness is given by

$$dR_p = \frac{\rho_p}{L} dx \tag{2}$$

where ρ_p is the sheet resistance in the p buffer layer beneath the n$^+$ adjusting region. The voltage drop caused by the current in dx is expressed by d$V_p(x)$. Therefore, the total voltage drop between point A to point B is as follows:

$$V_p(A) = \int_0^{W_n/2} dV_p dx = \int_0^{W_n/2} J_R \rho_p x dx = \frac{1}{8} J_R \rho_p W_n^2 \tag{3}$$

where W_n denotes the width of the n$^+$ adjusting region, and ρ_p can be expressed as [18, 23]

$$\rho_p = \frac{1}{q\mu_p[N_{ap} + p(t)]H_p} \tag{4}$$

where H_p is the depth of p buffer layer, N_{ap} is the doping concentration of p buffer layer, $p(t)$ is the hole density of p buffer layer during reverse recovery, μ_p is the hole mobility. The triggered condition of the parasitic npn transistor is as follows

$$V_p(t) = \frac{J_R(t)W_n^2}{8q\mu_p[N_{ap} + p(t)]H_p} \geq V_{bi} \approx 0.7\,\text{V} \tag{5}$$

Based upon the Eq. (5), it can be concluded that the injection efficiency of the npn transistor mainly depends on $J_R(t)$, W_n, N_{ap} and H_p.

3. Results and analyses

The diodes were simulated by the Sentaurus-TCAD software. Auger and Shockley-Read-Hall recombination models, carrier–carrier scattering, doping dependent and electric field dependent mobility models, and avalanche generation model were taken into account [3]. An over-stress condition with $V_{dc} = 2.5\,\text{kV}$, $J_F = 100\,\text{A/cm}^2$, $L = 1.25\,\mu\text{H}$ and $di/dt = 2000\,\text{A}/\mu\text{s}$ was considered during reverse recovery.
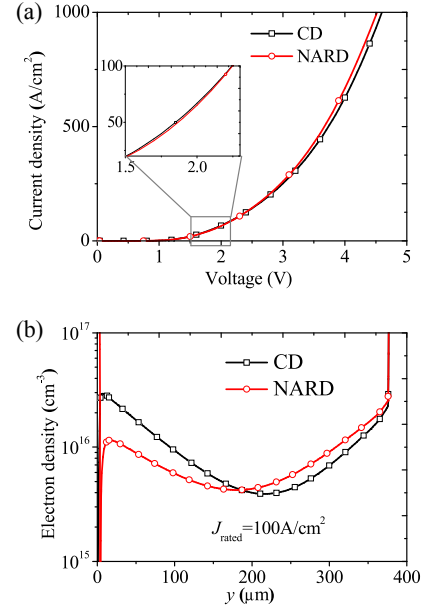

Fig. 2. (a) Comparison of forward conduction characteristics of two diodes. (b) Comparison of on-state electron density profiles ($x = 60\,\mu\text{m}$) at $J = J_{rated} = 100\,\text{A/cm}^2$.

Fig. 2(a) shows the forward conduction characteristics of two diodes. The carrier lifetimes in the simulation are adjusted to have the same forward voltage drop $V_F = 2.25\,\text{V}$ at the rated current density $J_{rated} = 100\,\text{A/cm}^2$. The carrier lifetimes for the conventional diode are $\tau_p = 0.5\,\mu\text{s}$ and $\tau_n = 2.5\,\mu\text{s}$, and for the NARD $\tau_p = 0.75\,\mu\text{s}$ and $\tau_n = 3.75\,\mu\text{s}$. Compared with the conventional diode, the forward voltage drop in the NARD increases below $J_{rated} = 100\,\text{A/cm}^2$ (shown in the illustration), due to the lower carrier density in front of the n$^+$ adjusting region. This leads to the inverted carrier profile, i.e., the carrier concentration of the cathode side is larger than the anode side, as shown in Fig. 2(b). It is critical to obtain the fast and soft recovery behavior [10].

Fig. 3 compares the reverse breakdown characteristics at $T = 300\,\text{K}$ and at $T = 400\,\text{K}$ in two diodes. The p buffer layer was carefully designed to prevent the electric field from punching through the n$^+$ adjusting region under static blocking condition. Therefore, the NARD has the same breakdown voltage as the conventional diode at the onset of static avalanche. However, it shows a lower leakage current both at room and high temperatures, because of larger carrier lifetimes in the n$^-$ base. Even under high avalanche current density, the NARD structure still exhibits the same positive and negative differential resistance branches as the conventional diode, which attributes to the buffer layers at both sides, leading to the improvement of static avalanche capability [24, 25, 26, 27].

The comparison of reverse recovery characteristics in two diodes are shown in Fig. 4. The dotted line represents the electron current density at the anode side during reverse recovery in the NARD. It shows that the parasitic npn transistor at the anode side is triggered at $t = 1.705\,\mu\text{s}$. Compared with the conventional diode, the NARD shows the faster reverse recovery with a reduced time of 40 ns and the lower reverse peak current density with a 21% reduc-
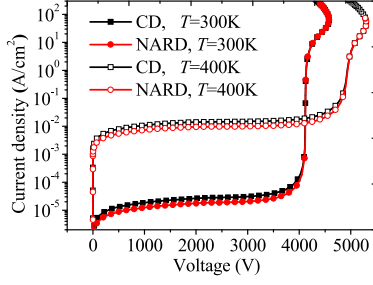
Fig. 3. Comparison of reverse breakdown characteristics at $T = 300\,\mathrm{K}$ and at $T = 400\,\mathrm{K}$ in two diodes.

tion. These are attributed to the lower on-state carriers stored in front of the p buffer layer and the less carriers generated by weak dynamic avalanche during reverse recovery in the NARD, and the less extracted holes compensated by the injected electrons of the npn transistor.
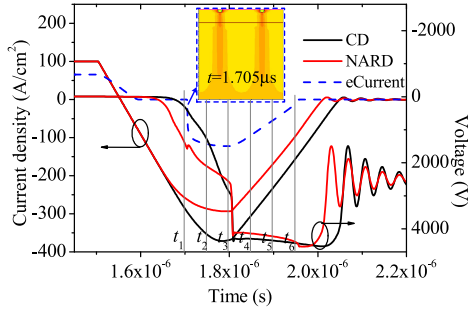

Fig. 4. Comparison of reverse recovery characteristics of two diodes during reverse recovery.

The dynamic avalanches are analyzed by the evolution of electric field distributions at different times in two diodes, as shown in Fig. 5. For the conventional diode, at the pn⁻ junction the electric field gradient in the n⁻ base region can be given by [28, 29]

$$\frac{\mathrm{d}E}{\mathrm{d}y} = \frac{q(N_\mathrm{D} + p + p_\mathrm{av})}{\varepsilon} \tag{6}$$

where p is the on-state holes, p_av is the avalanche generated holes, and N_D is the ionized donors in the n⁻ base region. This leads to a high peak electric field strength of $E_\mathrm{pn-} = 2.27 \times 10^5\,\mathrm{V/cm}$ at the pn⁻ junction at $t_4 = 1.85\,\mu\mathrm{s}$. A strong Egawa field [27, 30, 31] occurs, and this may lead to the diode failure. The electric field crowding is caused by the current filament generated by dynamic avalanche, because the electric field inside the current filament is higher [3, 4, 5, 6, 7]. For the NARD, however, electrons are injected by the npn transistor, and the electric field gradient is then given by

$$\frac{\mathrm{d}E}{\mathrm{d}y} = \frac{q(N_\mathrm{D} + p + p_\mathrm{av} - n)}{\varepsilon} \tag{7}$$

where n is the electrons injected by the npn transistor. The electrons compensate the holes injected on-state and generated by dynamic avalanche, resulting in the decrease of the peak electric field strength at the pn⁻ junction. In Fig. 5(b), at $t_1 = 1.7\,\mu\mathrm{s}$, the peak electric field strength at the pn⁻ junction reaches a maximum value $E_\mathrm{pn-} = 2.04 \times$

$10^5\,\mathrm{V/cm}$. Then it decreases dramatically after the npn transistor triggering at $t_2 = 1.75\,\mu\mathrm{s}$. As a result, the dynamic avalanche at the pn⁻ junction decreases. In the NARD, the less avalanche generated electrons at the pn⁻ junction move towards the cathode side, leading to a lower $E_\mathrm{nn-} = 1.48 \times 10^5\,\mathrm{V/cm}$ as well. This avoids the strong dynamic avalanches at both sides.
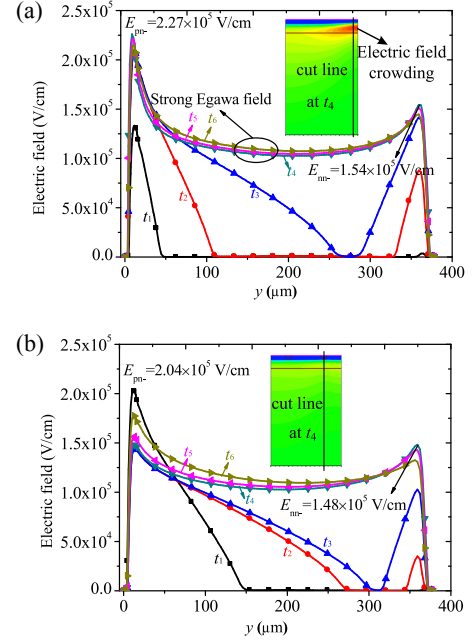

Fig. 5. Evolution of electric field distributions at different times in (a) the conventional diode ($x = 79\,\mu\mathrm{m}$) and in (b) the NARD ($x = 60\,\mu\mathrm{m}$).

Fig. 6 shows the dependence of the electron injection efficiency γ_n ($J_\mathrm{n}/J_\mathrm{R}$) on W_n, H_p and N_ap in the NARD. The electron injection efficiency γ_n of the npn transistor is determined by $V_\mathrm{p}(t)$ of Eq. (5). Hence, as explained in Eq. (5), γ_n is also depended on W_n, H_p and N_ap. It is obvious from this figure that γ_n increases with the increase of W_n, and decreases with the increases of H_p and N_ap. It also shows that the npn transistor is triggered into its on-state mode earlier for a increase in γ_n. In Fig. 6(b), the npn transistor maintains the turn-off state during reverse recovery when H_p increases to $19\,\mu\mathrm{m}$. These are in agree with Eq. (5).

The relationship between the electron injection efficiency (γ_n) and the peak electric field strength of pn⁻ junction at the anode side has been added, as shown in Fig. 7. For the conventional diode, with the carrier extraction of the n⁻ base, the peak electric field strength at the pn⁻ junction increases gradually. At $t_4 = 1.85\,\mu\mathrm{s}$, the electric field strength reaches the maximum of $E_\mathrm{pn-} = 2.27 \times 10^5\,\mathrm{V/cm}$, due to the current filament generated by dynamic avalanche. Then the peak electric field strength decreases.

For the NARD, the electric field strength reaches the maximum of $E_\mathrm{pn-} = 2.04 \times 10^5\,\mathrm{V/cm}$ before the electron injection ($t_1 = 1.7\,\mu\mathrm{s}$). The npn transistor is triggered at $t = 1.705\,\mu\mathrm{s}$, and the holes including that of on-state injection and the avalanche generation are compensated by injected electrons, leading to the decrease of peak electric
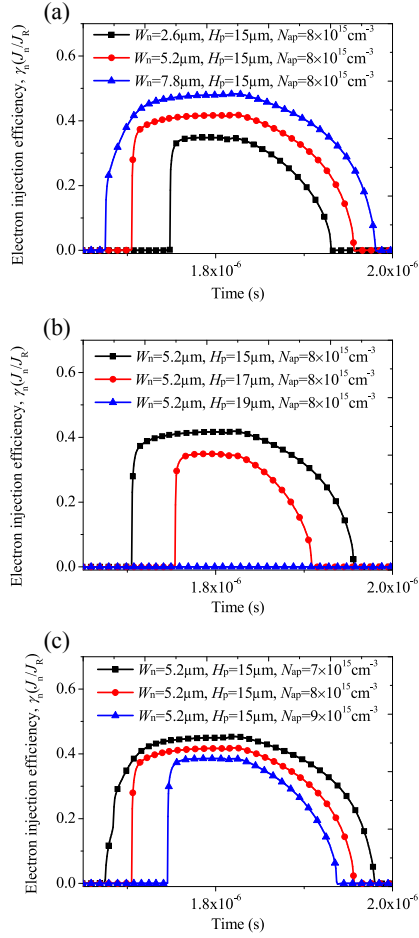
Fig. 6. Dependence of electron injection efficiency γ_n (J_n/J_R) on (a) W_n, (b) H_p and (c) N_{ap} in the NARD.
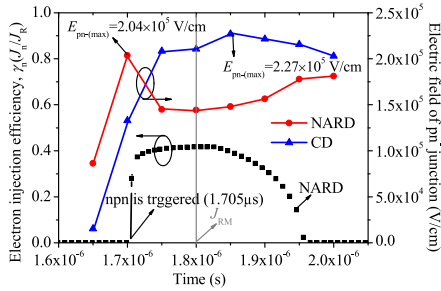

Fig. 7. The relationship between the electron injection efficiency (γ_n) and the peak electric field strength of pn^- junction in the NARD.

field. With the γ_n reaching the peak at $t_3 = 1.8\,\mu s$, the minimum of electric field strength occurs. Meanwhile, the reverse current density reaches its peak value (J_{RM}), and thereafter the plasma layer disappears. This leads to the rising of electric field distribution in the n^- base, provoking the peak electric field strength of the pn^- junction increases again.

4. Conclusion

A novel high voltage diode featuring partial n^+ adjusting region embedded at the anode side is proposed. The triggering condition of $V_p(t) \geqq 0.7\,V$ for the parasitic npn transistor is derived in relation to the parameters of W_n, H_p

and N_{ap}. The npn transistor is triggered with the increase of reverse current density during reverse recovery. The electrons are injected to compensate the holes at the pn^- junction. The simulations show that the peak electric fields decrease at both sides, and the dynamic avalanche capability is improved. Moreover, it shows a lower leakage current without sacrificing reverse blocking voltage.

Acknowledgments

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