

LETTER

# A high-pass filter based on through-silicon via (TSV)

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**Abstract** A fourth-order high-pass filter is proposed, which is formed by spiral inductors and TSV capacitors. The components of this filter rely on the TSV technology, which is generally regarded as vertical interconnection but now used to compose capacitor. The comparison of the results between finite element method and equivalent electric circuit obviously proves that they have nearly equal filtering characteristics including cut-off frequency and roll-drop rate. Moreover, the comparisons are made among the HPFs based on different technologies, and the challenges the proposed HPF faces are discussed.

**Keywords:** through-silicon via (TSV), high-pass filter, three-dimensional integrated circuit (3D IC)

**Classification:** Electron devices, circuits and modules

## 1. Introduction

Nowadays, the great progress is made in digital and analog circuits. However, there is still a big challenge in integrating radio frequency (RF) circuits, especially for the RF passive devices [1]. A key module of RF circuits is filter which consists of inductor, capacitor, and resistor. Those passive devices occupy much area, as a result the filter turns out to be hardly integrated, which makes researchers in great difficulty in practicing their systemic idea of interconnecting all modules together [2, 3, 4]. For resolving this problem, some kinds of techniques come out. One is through-silicon via (TSV) that is ordinarily termed as vertical interconnection [5, 6, 7, 8, 9]. The capacitor in terms of TSV is different from typical capacitor due to its small area and adapt to current IC manufactured process. The other technique is redistribution layer (RDL) [10, 11]. A planar spiral inductor is made in terms of RDL. In this letter, a novel fourth-order high-pass filter (HPF) of easy integration and small area is proposed [12, 13].

## 2. The TSV array capacitor and planar spiral inductor

The novel HPF is consistent in the ideal electronic HPF circuits given in Fig. 1 and modeled in advanced design system (ADS) an electronic design automation tool [14]. This fourth-order electronic HPF has two capacitors and inductors and superior filtering performance. The creative points are TSV-based capacitor and RDL-based inductor. The parameters of RC filter are as follows: the ideal

capacitances are 208 fF and 86 fF and the ideal inductances are 215 pH and 520 pH respectively. The possibility of making TSV-based capacitor successful depends on the structure of TSV that has an inner copper encompassed by silicon dioxide. The function of silicon dioxide is to insulate the copper from the silicon substrate [15, 16, 17, 18]. The topology structure of TSV arrays given in Fig. 2 is built in ANSYS Q3D Extractor a parasitic extraction tool for engineers designing electronic packaging and power electronic equipment [19]. The simulated capacitance value of TSV array1 and TSV array2 at the frequency of 20 GHz are 207.97 fF and 86.04 fF. Those values can be judged as ideal one.

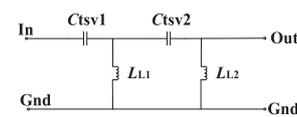


Fig. 1. The circuit of electronic.

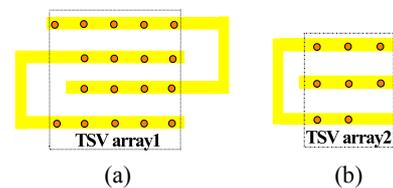


Fig. 2. (a) The topology structure of capacitor (207.97 fF) (b) The topology structure of capacitor (86.04 fF).

The model of RDL-based inductors makes in ANSYS Q3D Extractor. Note that the inductors should be surrounded by silicon dioxide for that gives them the practical circumstances. Like other planar spiral inductors, it consists of a RDL wound into a coil. The inductance is proportional to the turns [20, 21, 22, 23]. The final turns of four and three can satisfy inductances of 520 pH and 215 pH shown in Fig. 3. The simulated value of RDL inductances at the frequency of 20 GHz are 520.07 pH and 214.96 pH that can be treated as the ideal.

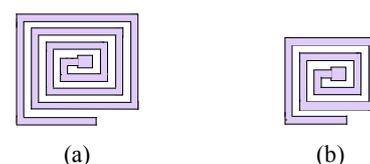


Fig. 3. (a) 4-turn inductor (520.07 pH) (b) 3-turn inductor (214.96 pH).

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### 3. HPF characteristics

The components of TSV HPF have been done by using technologies of TSV and RDL, and then interconnect all of them according to the ideal electronic HPF in HFSS “a finite element method solver for electromagnetic structures” [24].

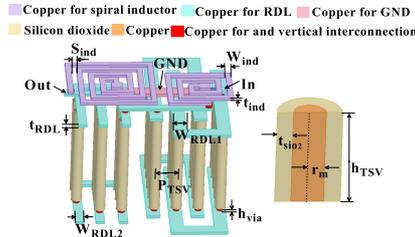


Fig. 4. The structure of TSV filter and cutaway view of cylindrical TSV.

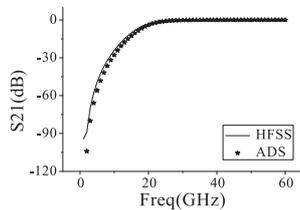


Fig. 5. The comparison between S-parameter of HFSS and that of ADS.

Table I. Structure parameters of proposed HPF

	Structure parameter	Symbol	Value ( $\mu\text{m}$ )
TSV capacitor	Radius of inner metal	$r_m$	4.7
	$\text{SiO}_2$ thickness	$t_{\text{SiO}_2}$	0.3
	Height	$h_{\text{TSV}}$	100
	Pitch	$p_{\text{TSV}}$	20
Inductor	Width of metal wires	$W_{\text{ind}}$	5
	Space between metal wires	$S_{\text{ind}}$	5
	Thickness	$t_{\text{ind}}$	3
RDL	Width	$W_{\text{RDL1}}$	12
	Width	$W_{\text{RDL2}}$	8
	Thickness	$t_{\text{RDL}}$	3
Via	Diameter	$d_{\text{via}}$	6
	Height	$h_{\text{via}}$	3

Fig. 4 vividly shows the structure of HPF and the cutaway view of TSV and all parameters of TSV filter can be found in Table I. The S-parameter of TSV filter obtained by HFSS and ADS tell that the electronic filter can be replaced fully by novel one for the nearly same filtering characteristics including cut-off frequency of 20 GHz and superior roll-drop rate, all which reflects well in Fig. 5. It is good to obtain a faultless substitute for passive filter and the substitute is easy to integrate and cover less area. Finally in order to illustrate the advantages of the proposed TSV filter, the Table II shows the comparison among HPFs based on different technologies. Accord-

ing to the data in Table II, the proposed HPF occupies the least area of  $0.16 \times 0.205 \text{ mm}^2$ , which is much more compact than the others.

Table II. Comparison with different HPFs

Filter	Cutoff frequency (GHz)	Size ( $\text{mm}^2$ )	Technology
[25]	0.07	$32 \times 10$	Microstrip line
[26]	2.3	$87.5 \times 12.0$	Microstrip & Transmission Zero
[27]	1	$5.8 \times 4.2$	Liquid crystal polymer (LCP)
This work	20	$0.16 \times 0.205$	TSV & RDL

### 4. Further discussion

Although the proposed filter has advantages of small size and good characteristics, two aspects of challenges need to be considered [28, 29, 30]. One is 3D packaging for radio-frequency circuits. The proposed TSV-based HPF, fabricated in 3D packaging, would be affected severely by the noise from the adjacent module through silicon substrate in radio frequency. So the electromagnetic interference should be shield effectively. The other is the side effect of technology development. In new 3D chips, TSVs will have smaller dimensions, including smaller radius, height, oxide liner thickness, and TSV-to-TSV pitch. Firstly, because of smaller radius and height of TSV, the lateral surface area of TSV would shrink, which leads to smaller coupling capacitance between two TSVs. Secondly, due to the smaller oxide liner thickness and TSV-to-TSV pitch, the distance between two plates of capacitor is decreased, which results in larger capacitance between TSVs. Therefore, the capacitor based on TSV array should be redesigned with the development of technology.

### 5. Conclusion

The outcome of comparing indicates that the TSV filter possesses almost same filtering function and the area of that is much smaller. So this proposed filter with such good qualities should be given more attention and will provide more brief resolutions for electronic industry in the days to come. At the same time the challenges that the proposed HPF faces are further discussed, including 3D packaging for radio-frequency circuits and the side effect of technology development.

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### References

- [1] F. J. Wang, *et al.*: “A low-pass filter made up of the cylindrical through-silicon-via,” 19th International Conference on Electronic Packaging Technology (ICEPT) (2018) 257 (DOI: 10.1109/ICEPT.2018.8480573).
- [2] J. Cheng, *et al.*: “Integrated passive devices on through silicon interposer with re-distribution layers,” IEEE 16th Electronics

- Packaging Technology Conference (EPTC) (2014) 265 (DOI: 10.1109/EPTC.2014.7028270).
- [3] K. Zoschke, *et al.*: “Thin film integration of passives-single components, filters, integrated passive devices,” Proc. 54th Electronic Components and Technology Conference **1** (2004) 294 (DOI: 10.1109/ECTC.2004.1319354).
  - [4] C. C. Mao, *et al.*: “Design of LC bandpass filters based on silicon-based IPD technology,” 19th International Conference on Electronic Packaging Technology (ICEPT) (2018) 238 (DOI: 10.1109/ICEPT.2018.8480419).
  - [5] F. J. Wang, *et al.*: “A novel guard method of through-silicon via (TSV),” IEICE Electron. Express **15** (2018) 20180421 (DOI: 10.1587/ele.15.20180421).
  - [6] X. K. Yin, *et al.*: “Metal proportion optimization of annular through-silicon via considering temperature and keep-out zone,” IEEE Trans. Compon. Packag. Manuf. Technol. **5** (2015) 1093 (DOI: 10.1109/TCPMT.2015.2446768).
  - [7] L. Qian, *et al.*: “Electrical modeling and analysis of a mixed carbon nanotube based differential through silicon via in 3D integration,” IEEE Trans. Nanotechnol. **15** (2016) 155 (DOI: 10.1109/TNANO.2015.2509019).
  - [8] X. X. Liu, *et al.*: “Low-loss air-cavity through-silicon vias (TSVs) for high speed three-dimensional integrated circuits (3-D ICs),” IEEE Microw. Wireless Compon. Lett. **26** (2016) 89 (DOI: 10.1109/LMWC.2016.2517325).
  - [9] Q. J. Lu, *et al.*: “Electrical modeling and characterization of shield differential through-silicon vias,” IEEE Trans. Electron Devices **62** (2015) 1544 (DOI: 10.1109/TED.2015.2410312).
  - [10] X. K. Yin, *et al.*: “Effectiveness of p+ layer in mitigating substrate noise induced by through-silicon via for microwave applications,” IEEE Microw. Wireless Compon. Lett. **26** (2016) 687 (DOI: 10.1109/LMWC.2016.2597218).
  - [11] Q. J. Lu, *et al.*: “Accurate formulas for the capacitance of tapered-through silicon vias in 3-D ICs,” IEEE Microw. Wireless Compon. Lett. **24** (2014) 294 (DOI: 10.1109/LMWC.2014.2309075).
  - [12] F. J. Wang, *et al.*: “An ultracompact butterworth low-pass filter based on coaxial through-silicon vias,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25** (2017) 1164 (DOI: 10.1109/TVLSI.2016.2620460).
  - [13] X. K. Yin, *et al.*: “Ultra-compact TSV-based L-C low-pass filter with stopband up to 40 GHz for microwave application,” IEEE Trans. Microw. Theory Techn. **67** (2019) 738 (DOI: 10.1109/TMTT.2018.2882809).
  - [14] ADS software (2018) <http://www.keysight.com/en/pc-1297113/advanced-design-system-ads>.
  - [15] K. Ali, *et al.*: “Different scenarios for estimating coupling capacitances of through silicon via (TSV) arrays,” 5th International Conference on Energy Aware Computing Systems & Applications **90** (2015) 1 (DOI: 10.1109/ICEAC.2015.7352170).
  - [16] T. Ramadan, *et al.*: “Coupling capacitance extraction in through-silicon via (TSV) arrays,” IEEE International Conference on Electronics, Circuits, and Systems (ICECS) (2015) 470 (DOI: 10.1109/ICECS.2015.7440350).
  - [17] Y. Lin and C. S. Tan: “Physical and electrical characterization of 3D embedded capacitor: A high-density MIM capacitor embedded in TSV,” IEEE 67th Electronic Components and Technology Conference (ECTC) (2017) 1956 (DOI: 10.1109/ECTC.2017.45).
  - [18] S. H. Luo, *et al.*: “Novel LC resonant clocking for 3D IC using TSV-inductor and capacitor,” IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS) (2017) 1 (DOI: 10.1109/EDAPS.2017.8277019).
  - [19] Q3D Extractor software (2018) <http://www.ansys.com/Products/Electronics/ANSYS-Q3D-Extractor>.
  - [20] S. L. Gou, *et al.*: “Accurate inductance modeling of 3-D inductor,” IEEE Microw. Wireless Compon. Lett. **900** (2018) (DOI: 10.1109/LMWC.2018.2867089).
  - [21] C. Jin, *et al.*: “Integrated passive devices on through silicon interposer with re-distribution layers,” IEEE 16th Electronics Packaging Technology Conference (EPTC) (2014) 265 (DOI: 10.1109/EPTC.2014.7028270).
  - [22] X. H. Bian, *et al.*: “Simulation and modeling of wafer level silicon-base spiral inductor,” 13th International Conference on Electronic Packaging Technology & High Density (2012) 29 (DOI: 10.1109/ICEPT-HDP.2012.6474561).
  - [23] C. Zhuo, *et al.*: “System-level design consideration and optimization of through-silicon via inductor,” Integration (2017) (DOI: 10.1016/j.vlsi.2017.07.002).
  - [24] HFSS software (2018) <http://www.ansys.com/Products/Electronics/ANSYS-HFSS>.
  - [25] Y. J. Huang, *et al.*: “A compact, high-selectivity, and wide passband semi-lumped 70 MHz high-pass filter,” IEEE Asia Pacific Microwave Conference (APMC) (2017) 730 (DOI: 10.1109/APMC.2017.8251550).
  - [26] S. Parvez, *et al.*: “A novel quasi-lumped UWB high pass filter with multiple transmission zeros,” IEEE International Conference on Electrical Computer and Communication Engineering (ECCE) (2017) 895 (DOI: 10.1109/ECACE.2017.7913030).
  - [27] S. Qian, *et al.*: “Design and fabrication of a miniature high-pass filter using multilayer LCP technology,” IEEE 41st European Microwave Conference (2011) 187 (DOI: 10.23919/EuMC.2011.6101685).
  - [28] K. Zoschke, *et al.*: “Fabrication of application specific integrated passive devices using wafer level packaging technologies,” IEEE Trans. Adv. Packag. **30** (2007) 359 (DOI: 10.1109/TADVP.2007.901770).
  - [29] Q. Liu, *et al.*: “The development of electric coupling for RF IC package substrate,” 18th International Conference on Electronic Packaging Technology (ICEPT) (2017) 30 (DOI: 10.1109/ICEPT.2017.8046401).
  - [30] B. G. Kim, *et al.*: “Development on integrated passive devices using wafer level package technologies,” 12th Electronics Packaging Technology Conference (2010) 691 (DOI: 10.1109/EPTC.2010.5702727).